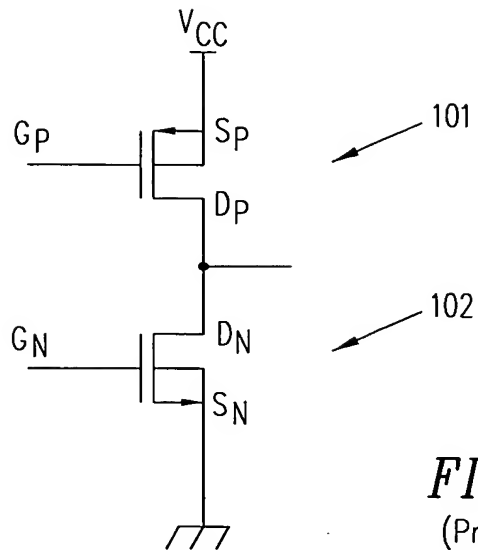
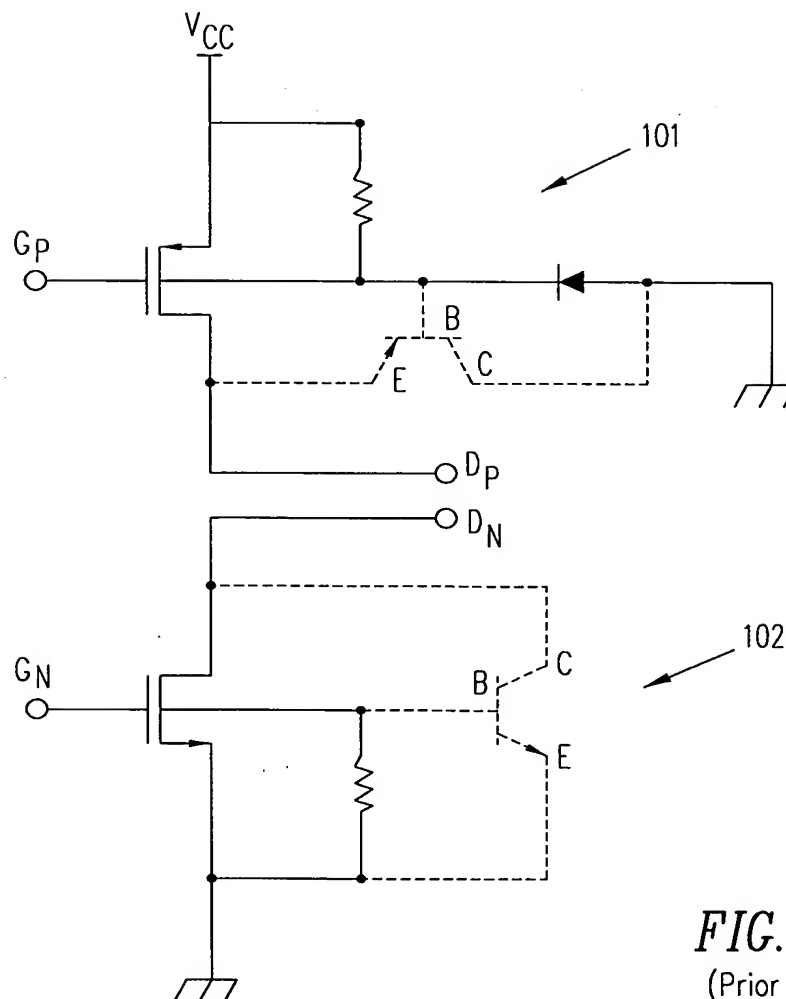


FIG. 1A  
(Prior Art)

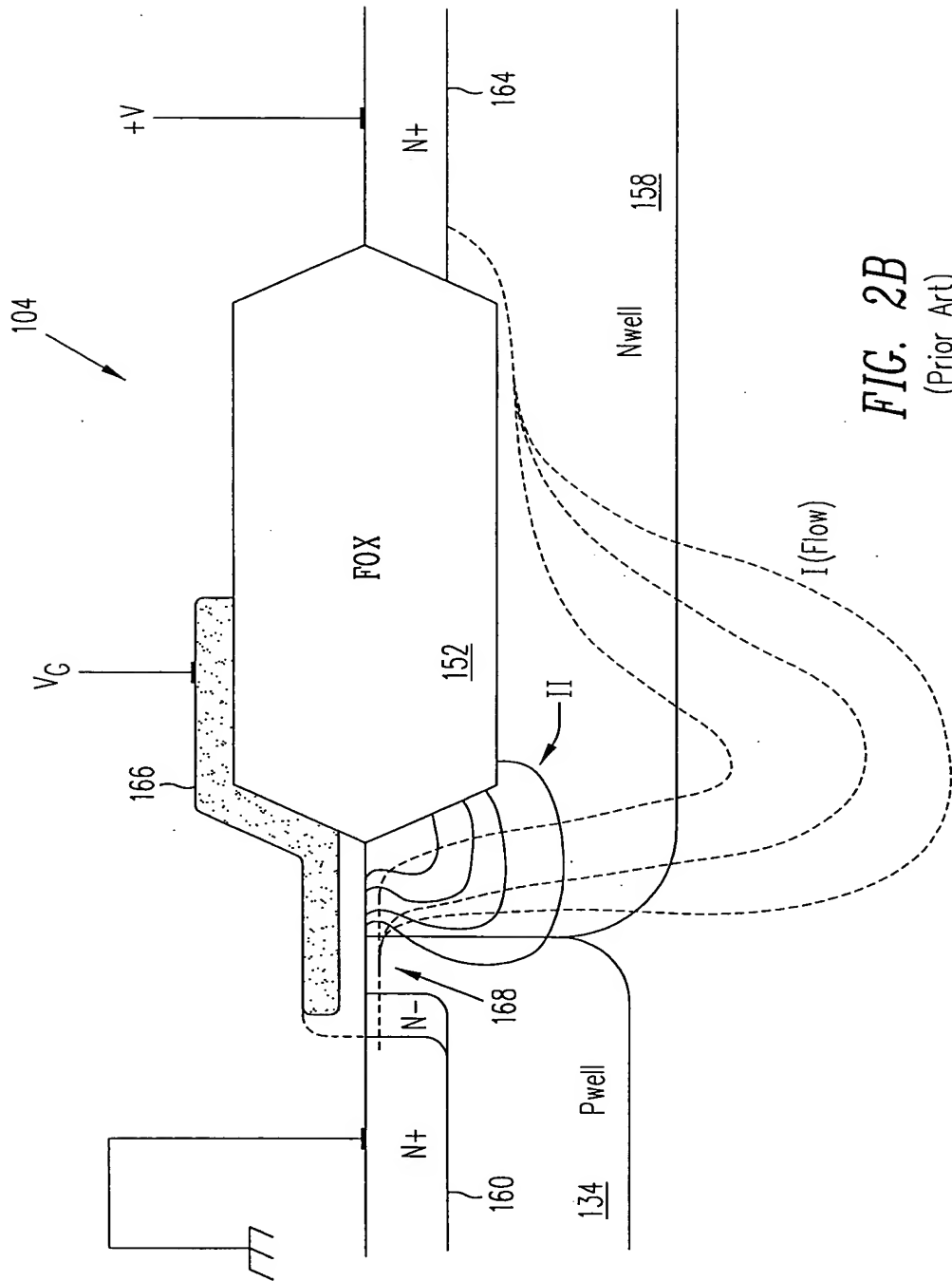


**FIG. 1B**  
(Prior Art)



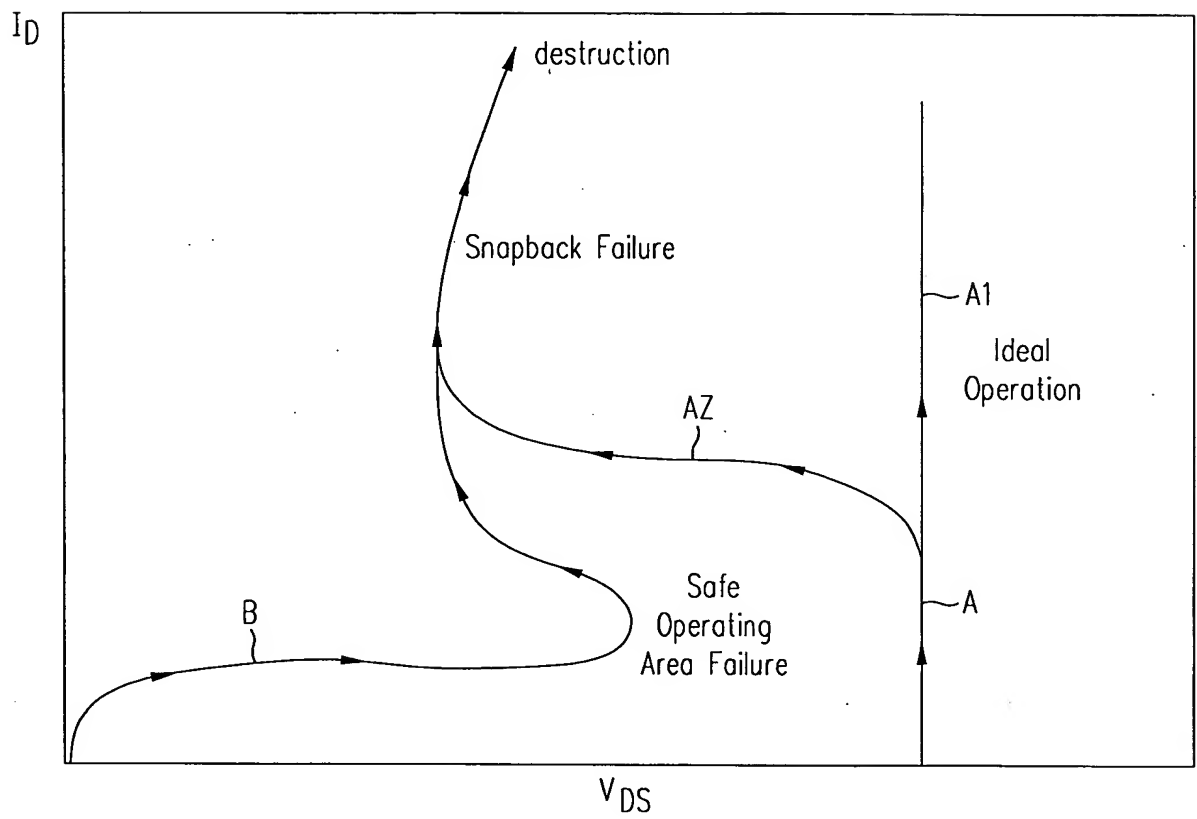
**FIG. 1C**  
(Prior Art)

FIG. 2A  
(Prior Art)



**FIG. 2B**  
(Prior Art)





**FIG. 2C**  
(Prior Art)

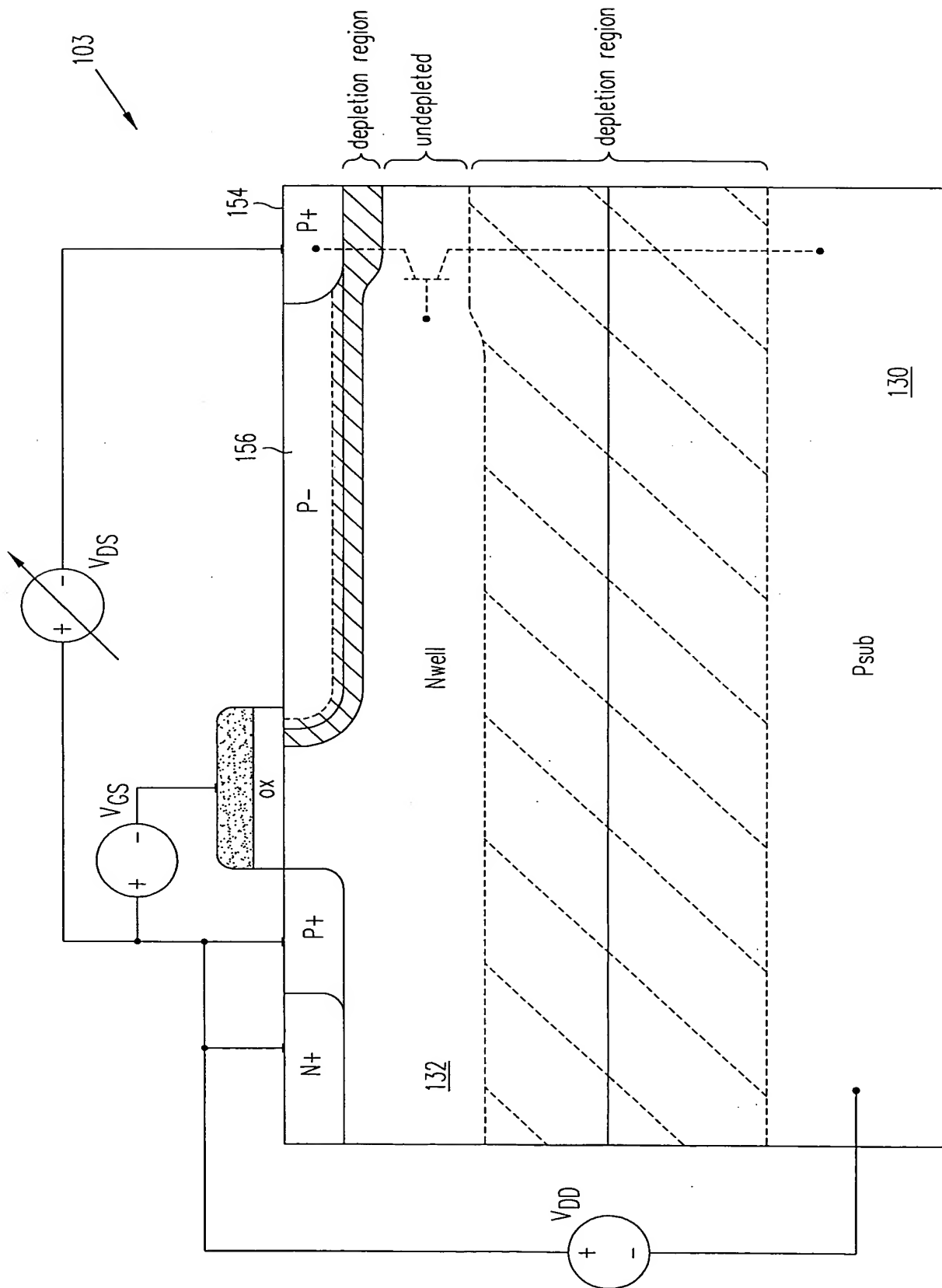


FIG. 2D (Prior Art)

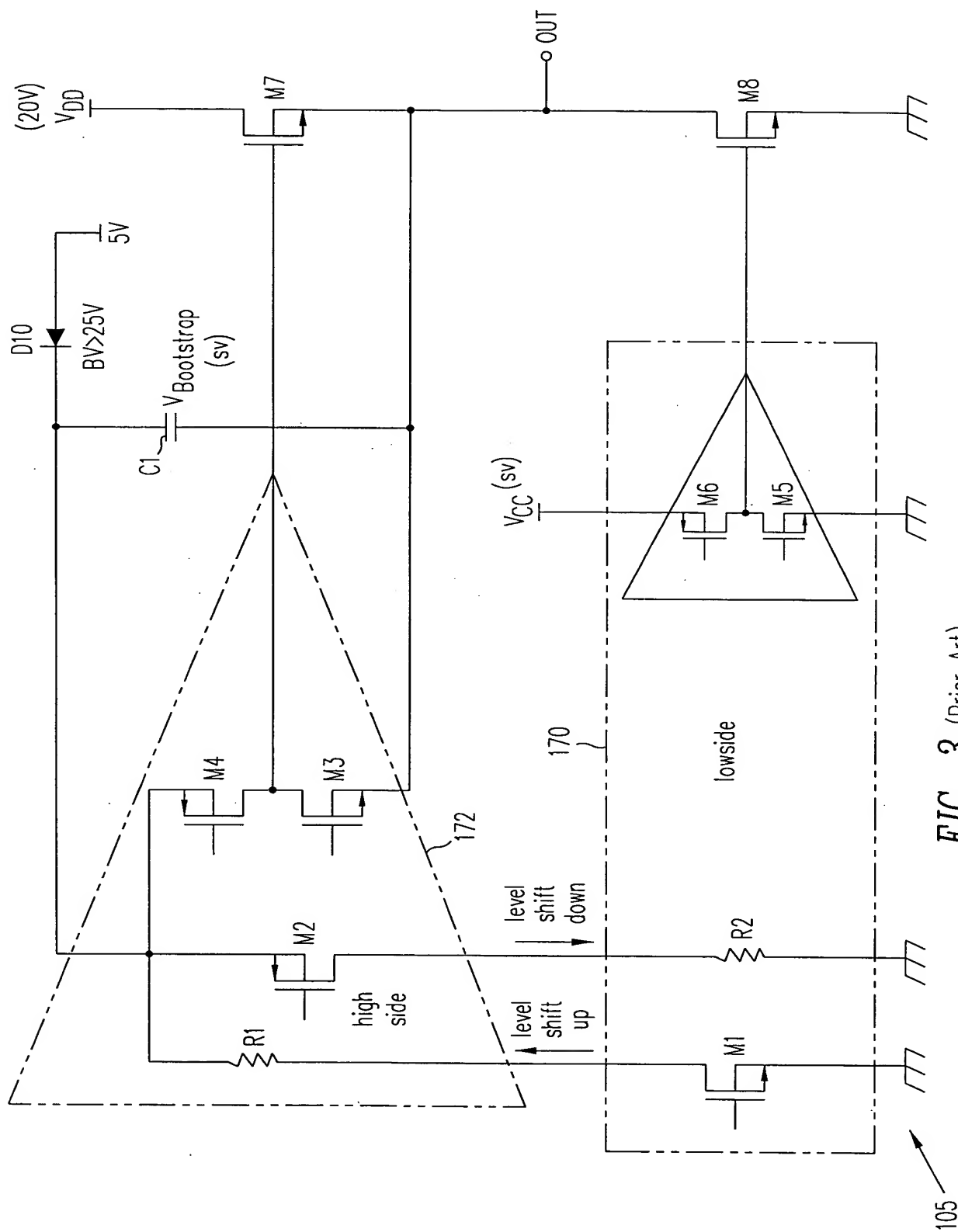


FIG. 3 (Prior Art)

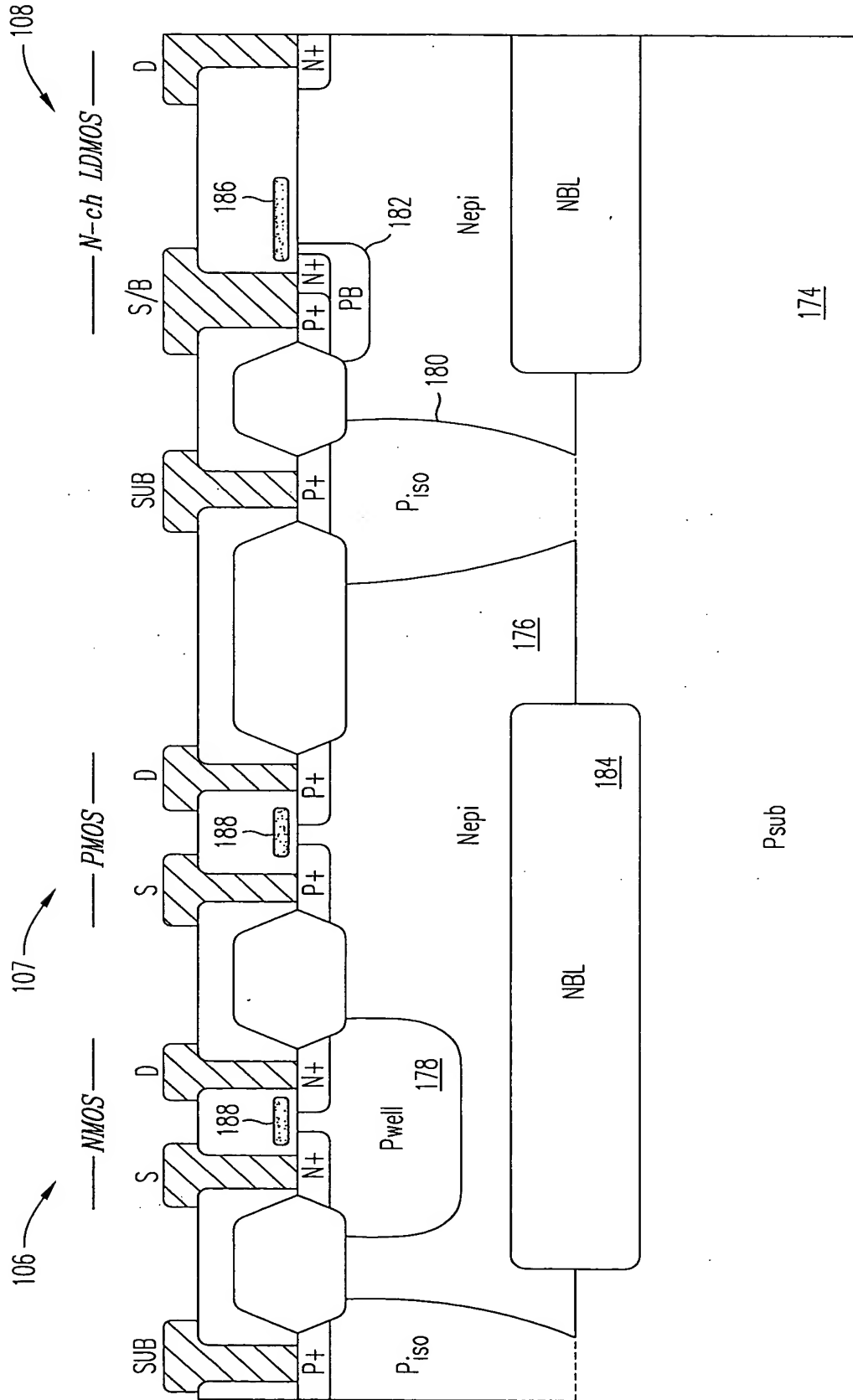


FIG. 4A  
(Prior Art)

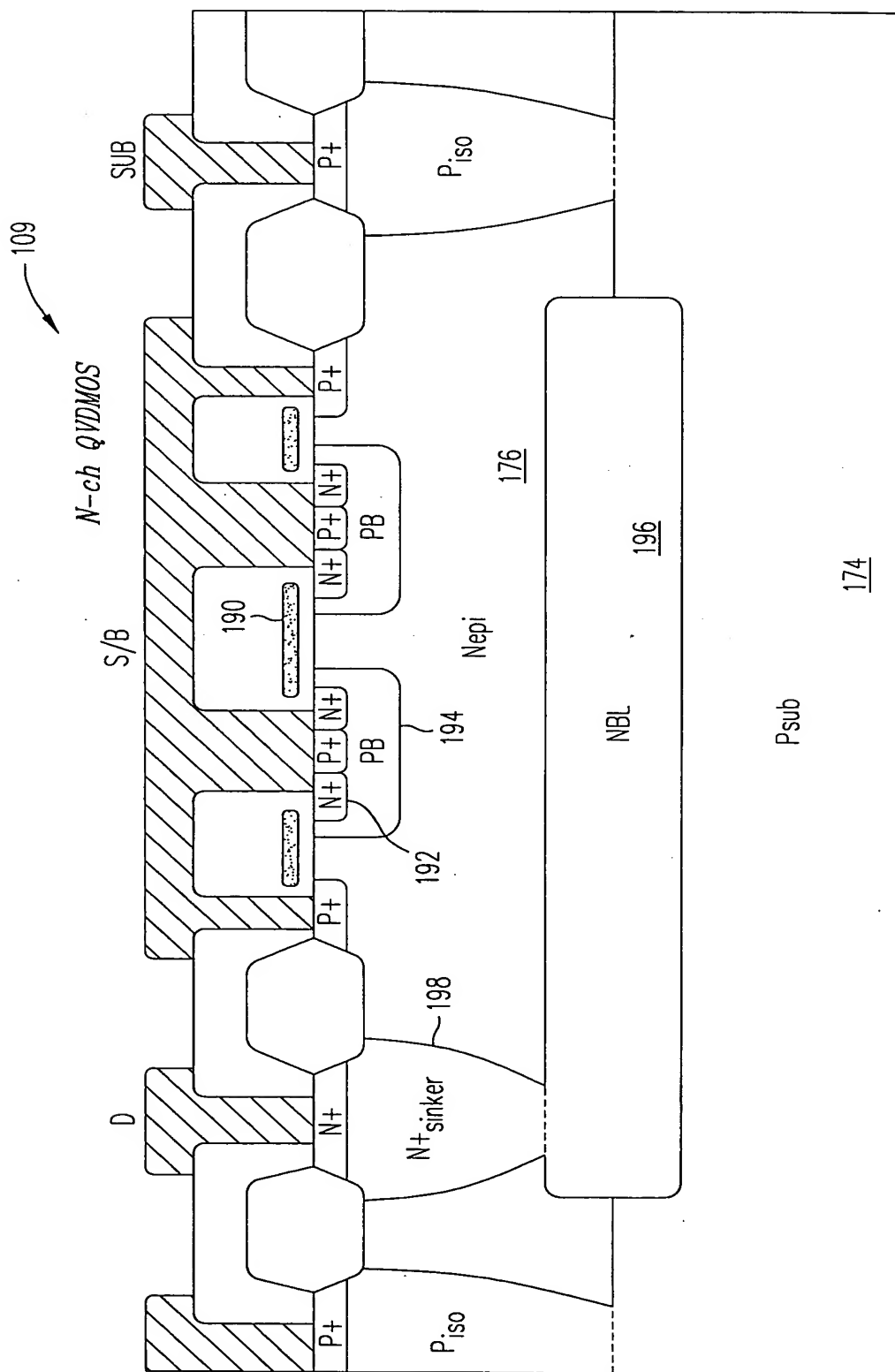
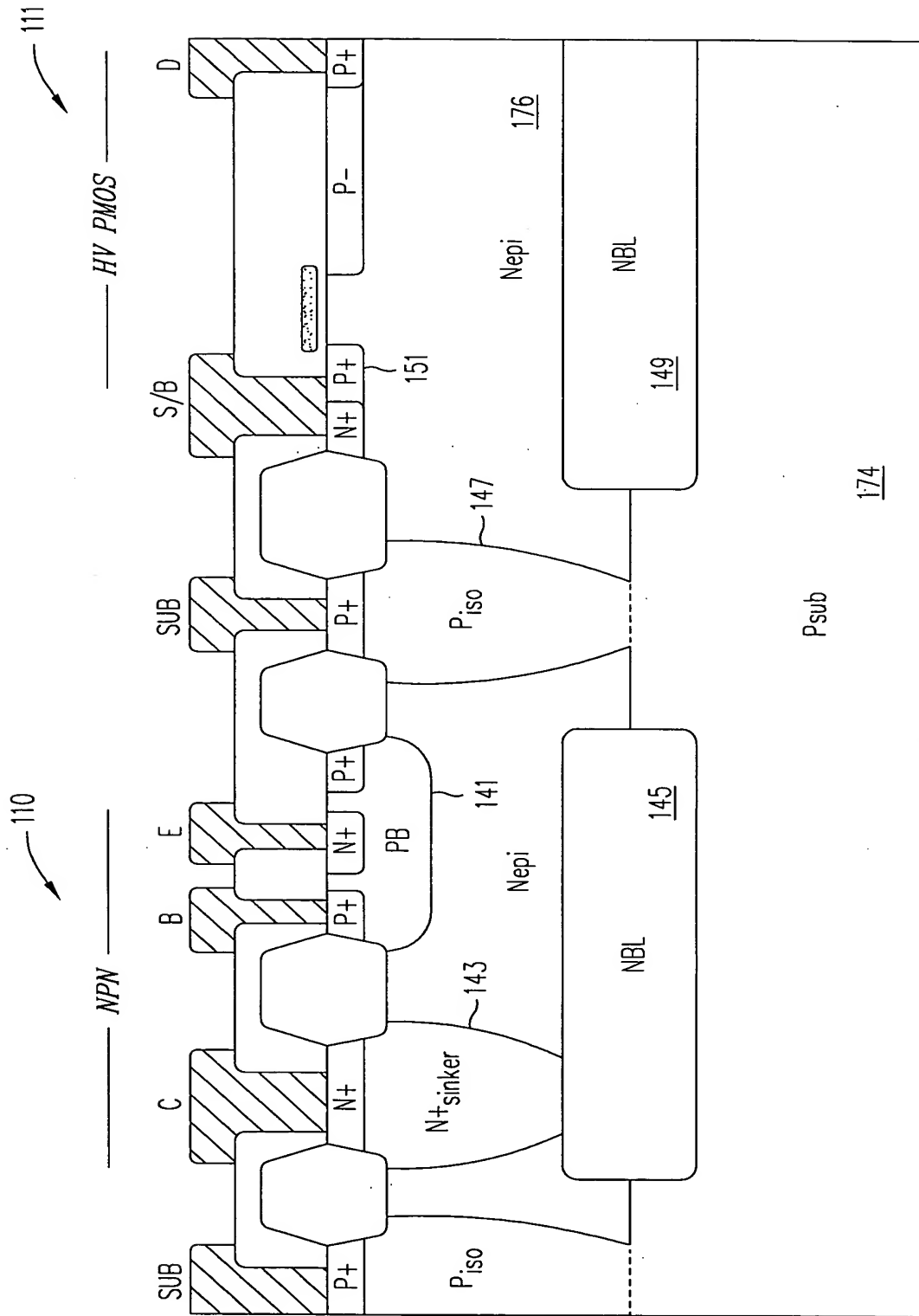
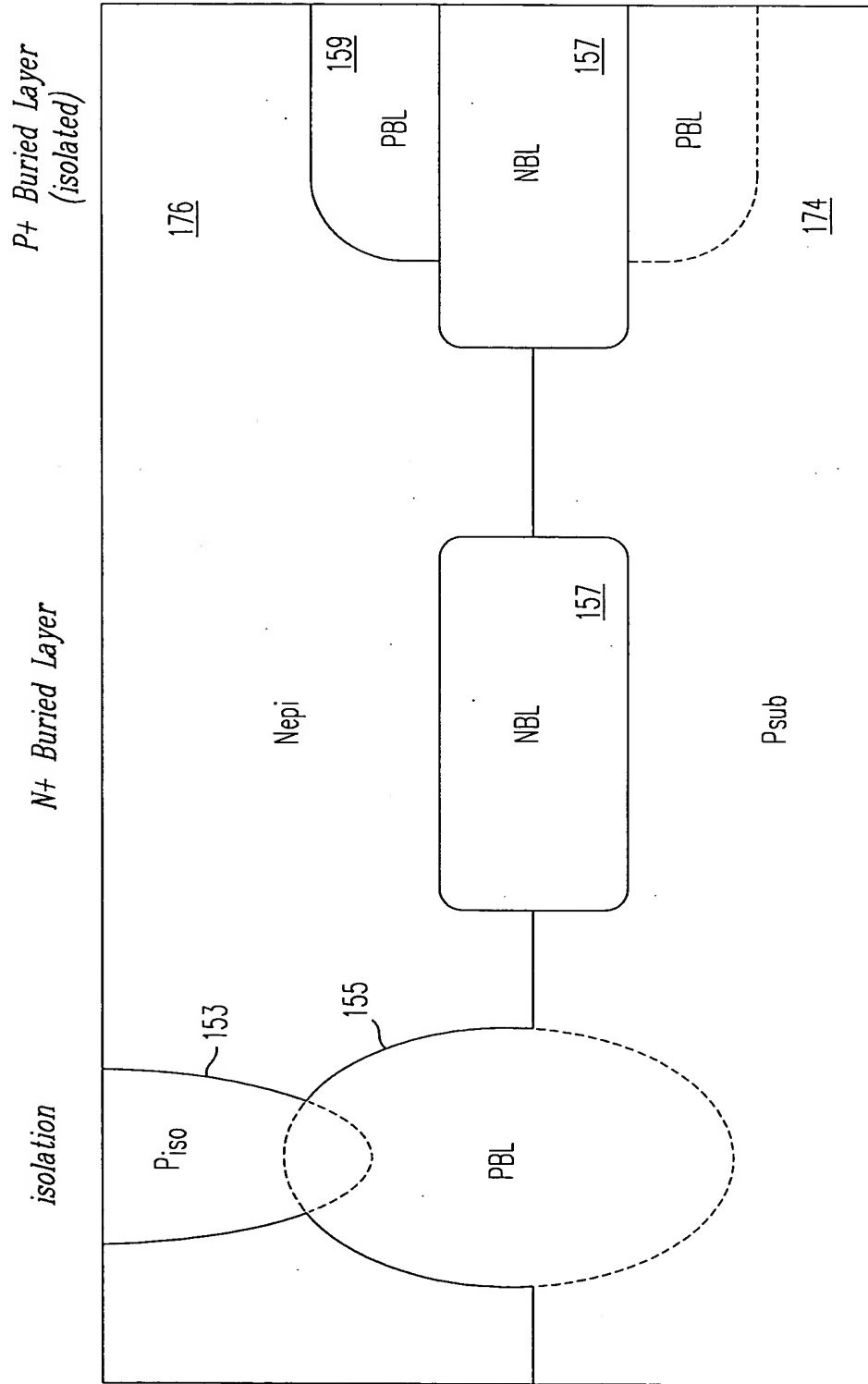


FIG. 4B  
(Prior Art)



**FIG. 4C**  
(Prior Art)



**FIG. 5A**

(Prior Art)





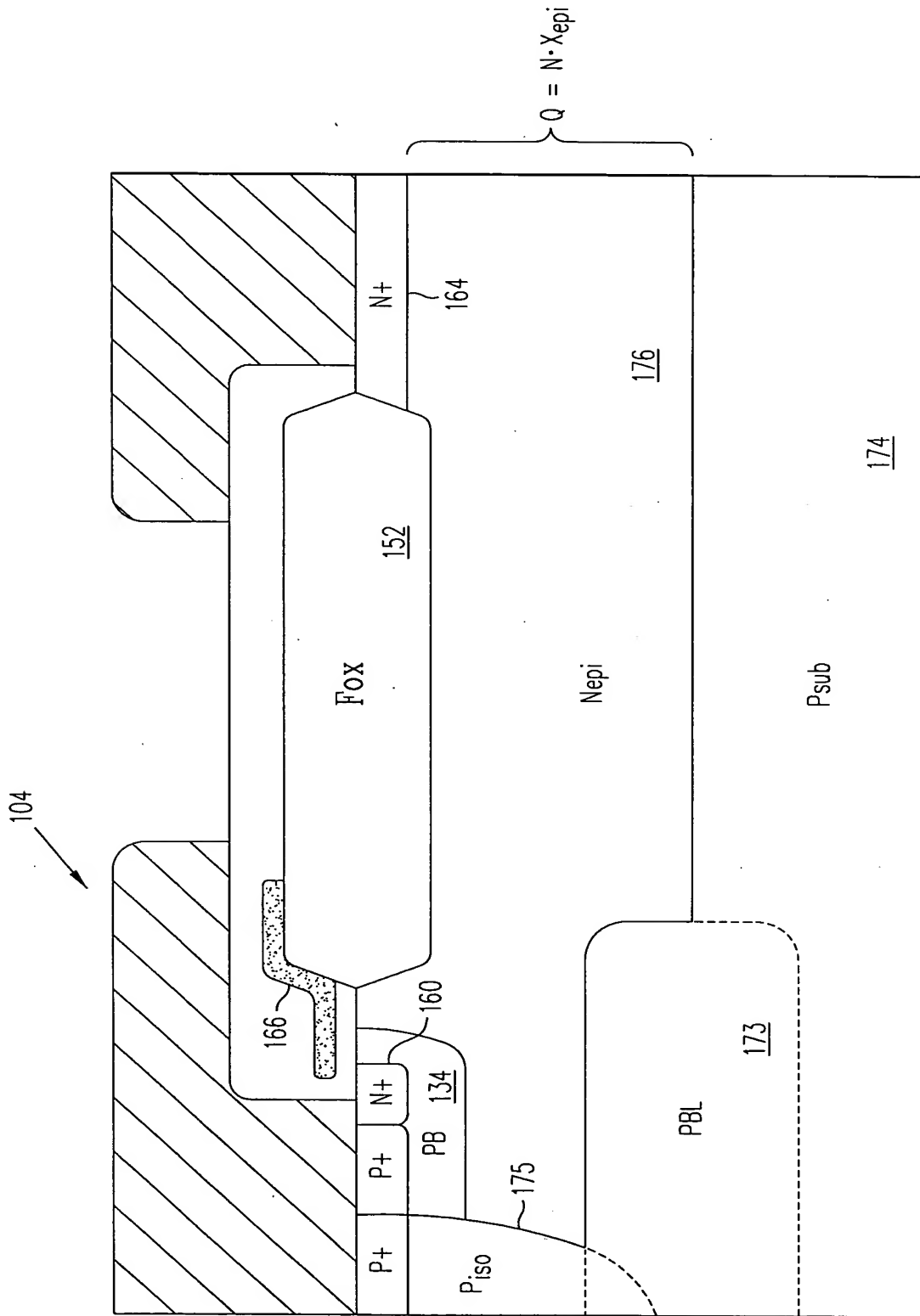
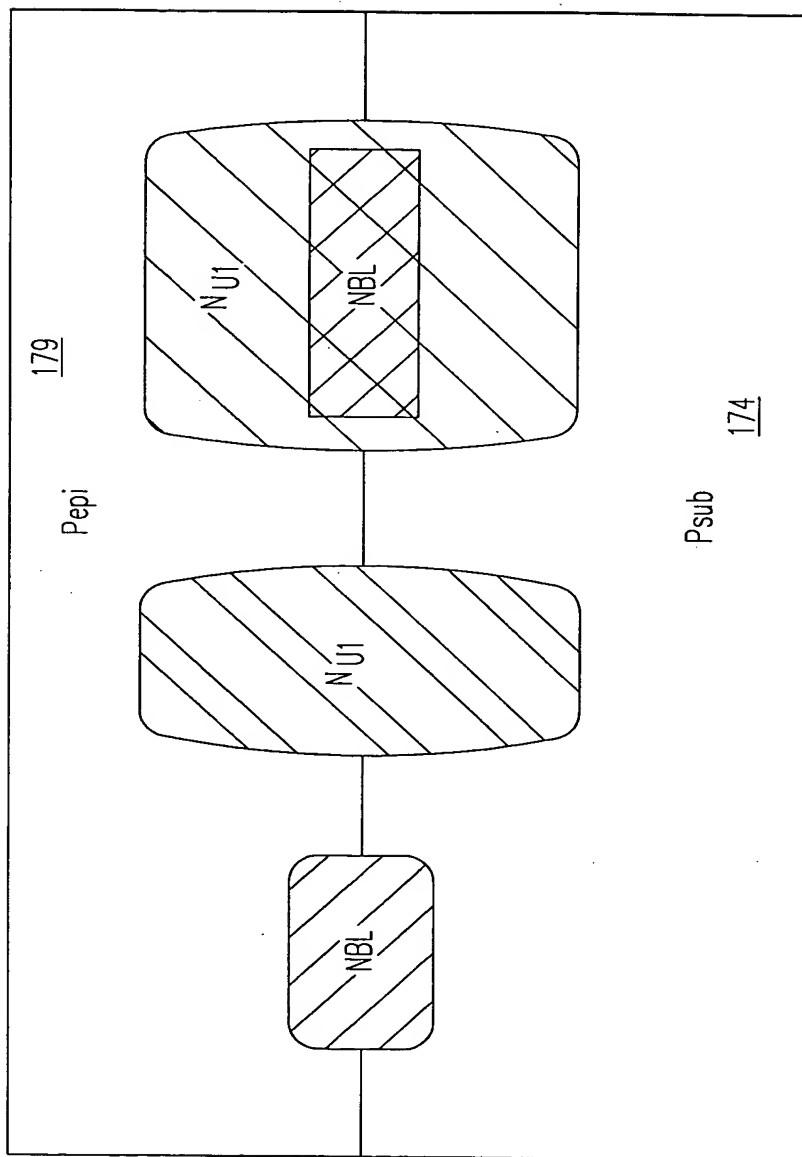


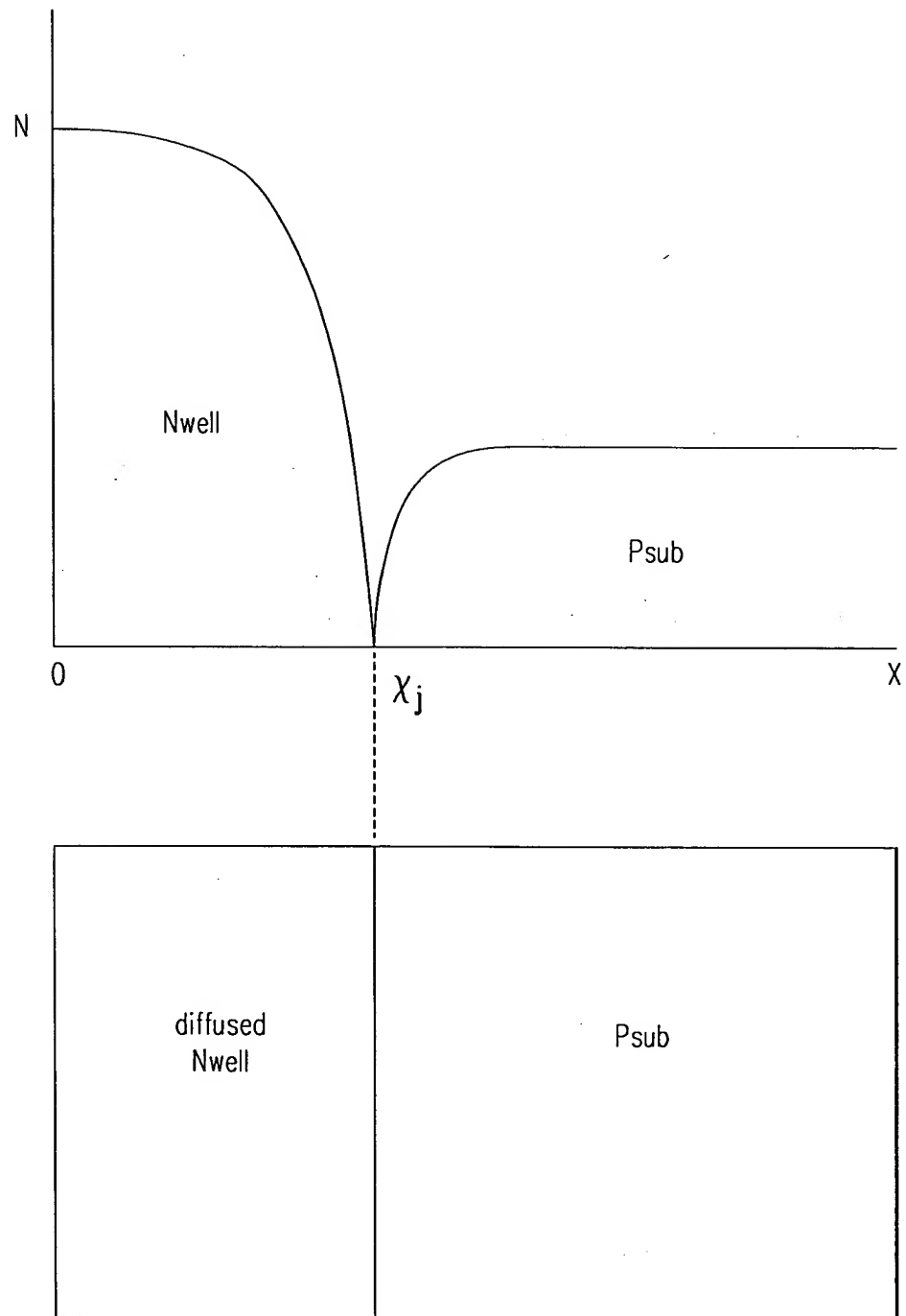
FIG. 5C  
(Prior Art)

FIG. 6A (Prior Art)

**FIG. 6B** (Prior Art)



**FIG. 6C**  
(Prior Art)



**FIG. 7A**  
(Prior Art)

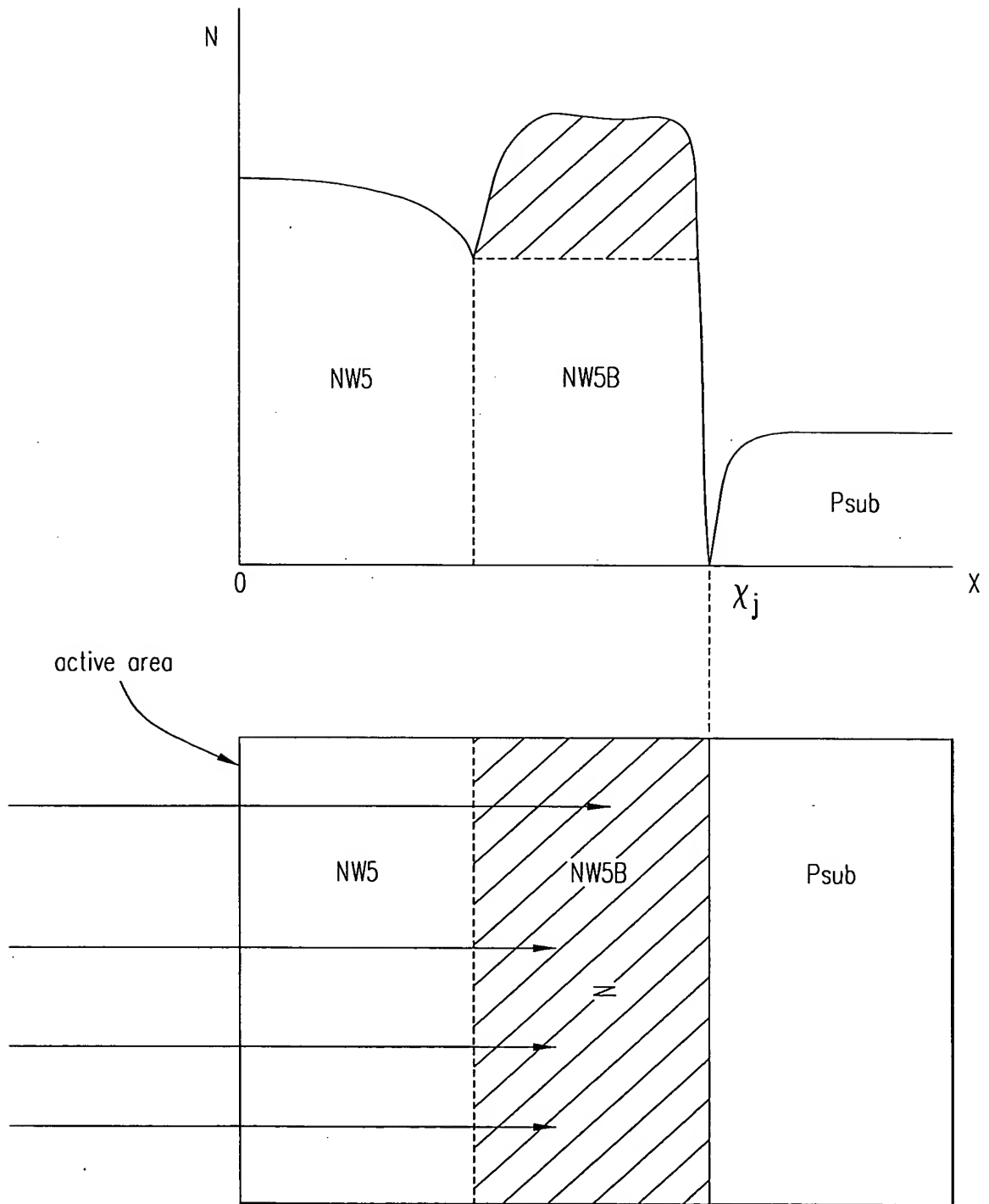


FIG. 7B

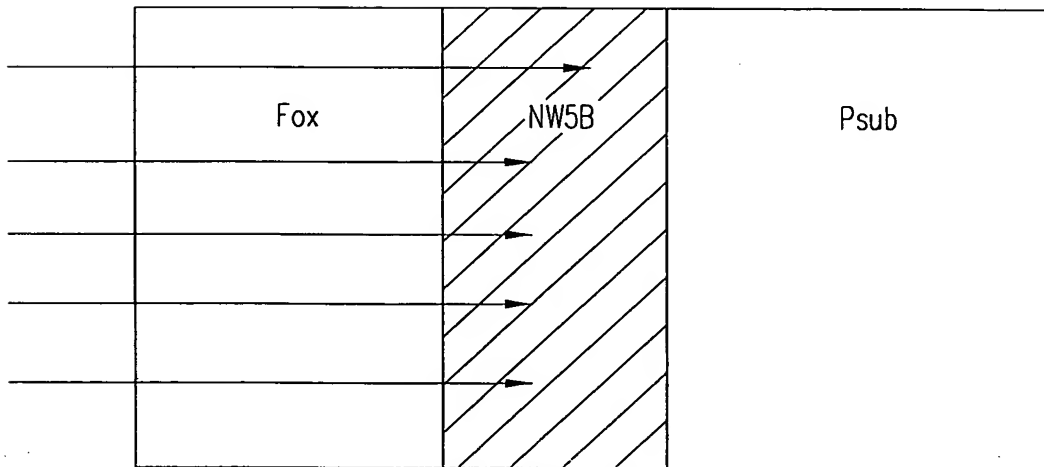
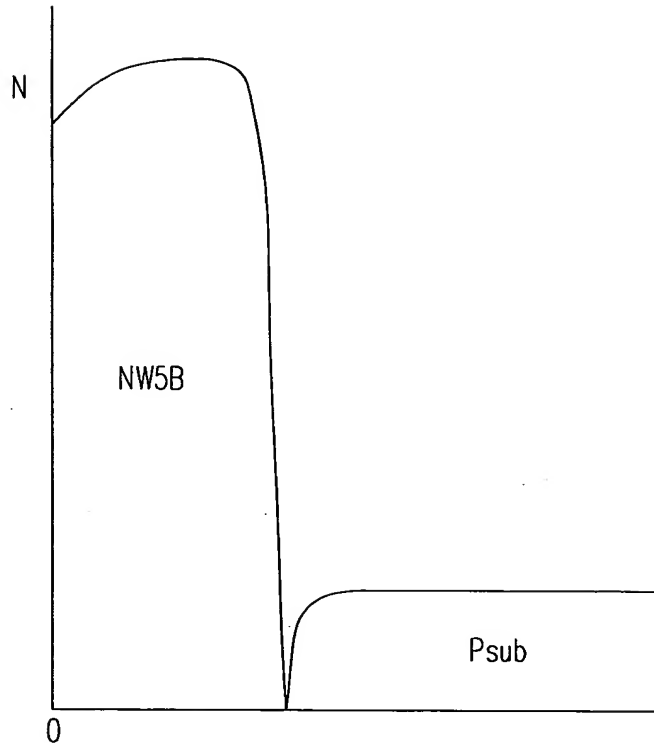


FIG. 7C

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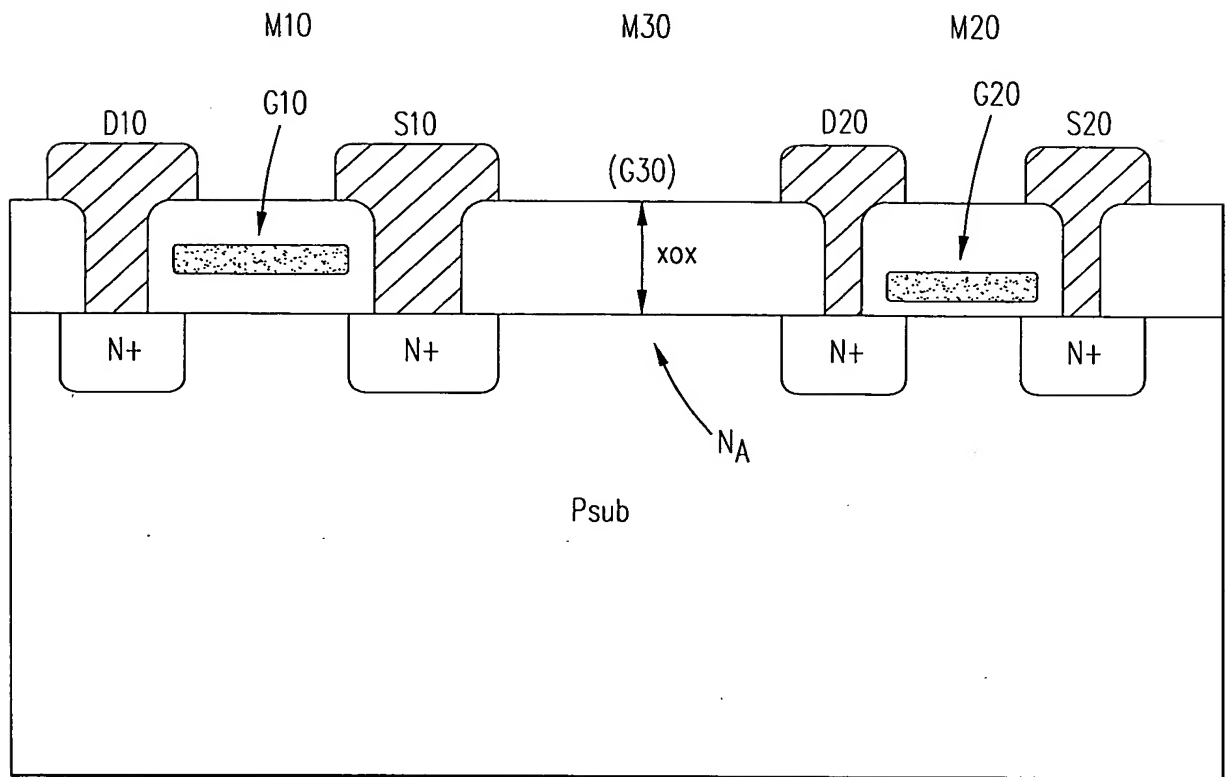


FIG. 8A

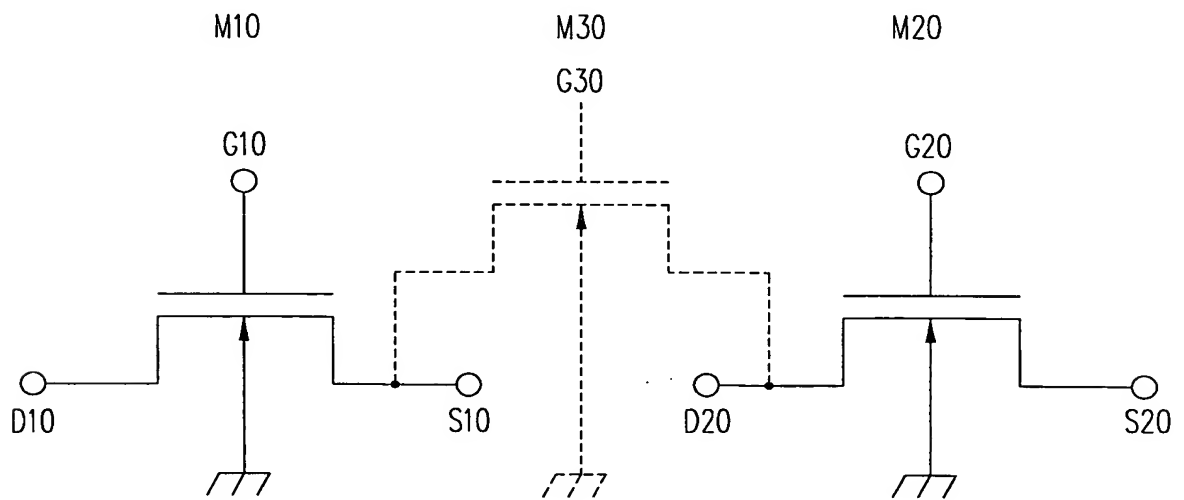


FIG. 8B



FIG. 9A  
(Prior Art)

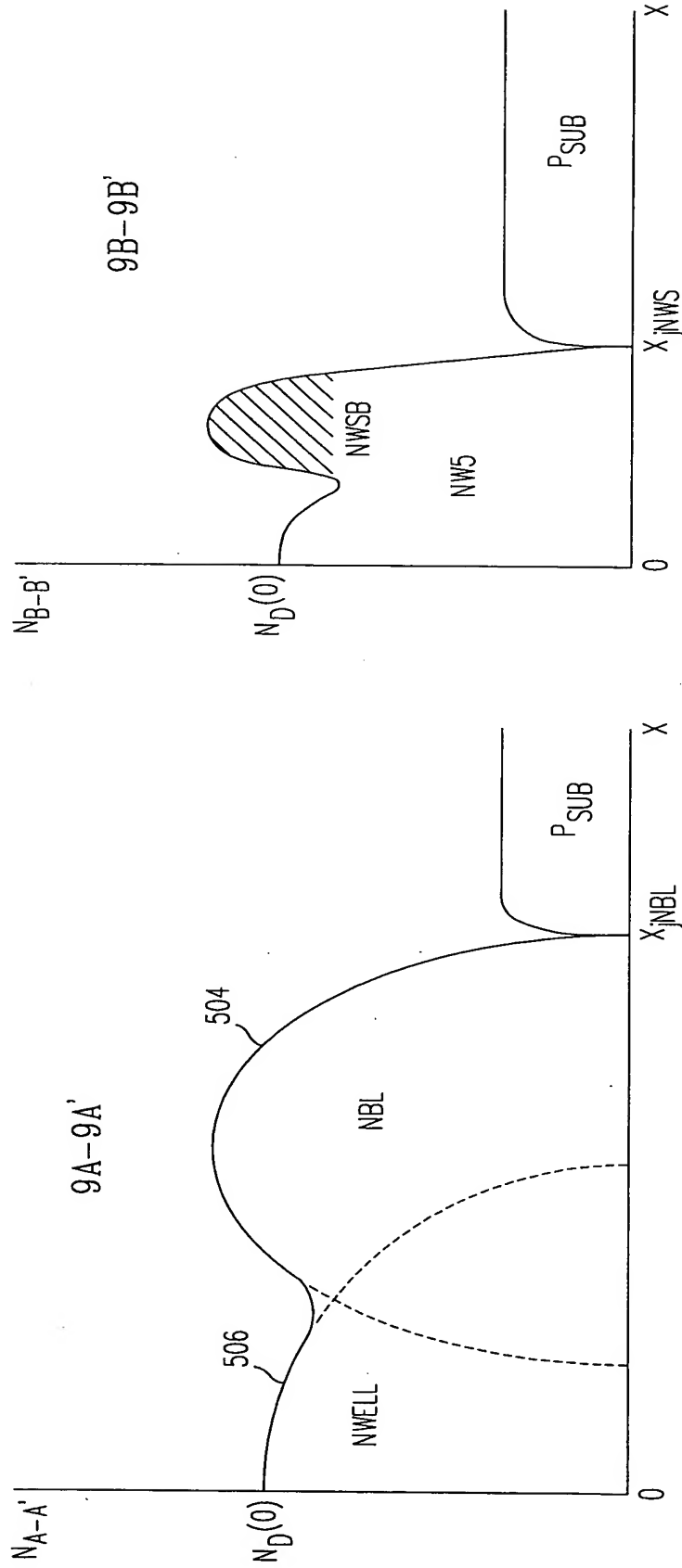


FIG. 9D  
(Prior Art)

FIG. 9C  
(Prior Art)

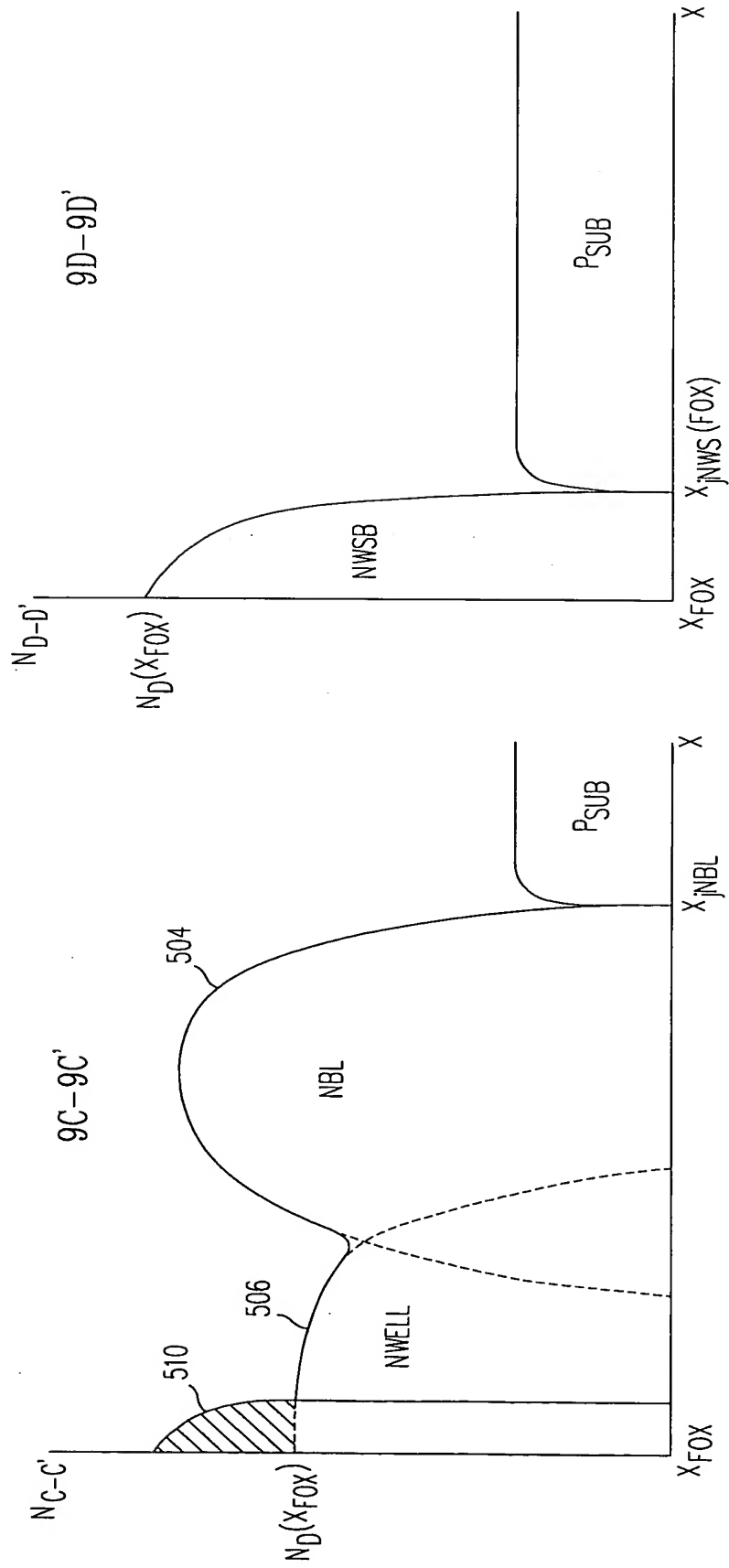


FIG. 9F  
(Prior Art)

FIG. 9E  
(Prior Art)

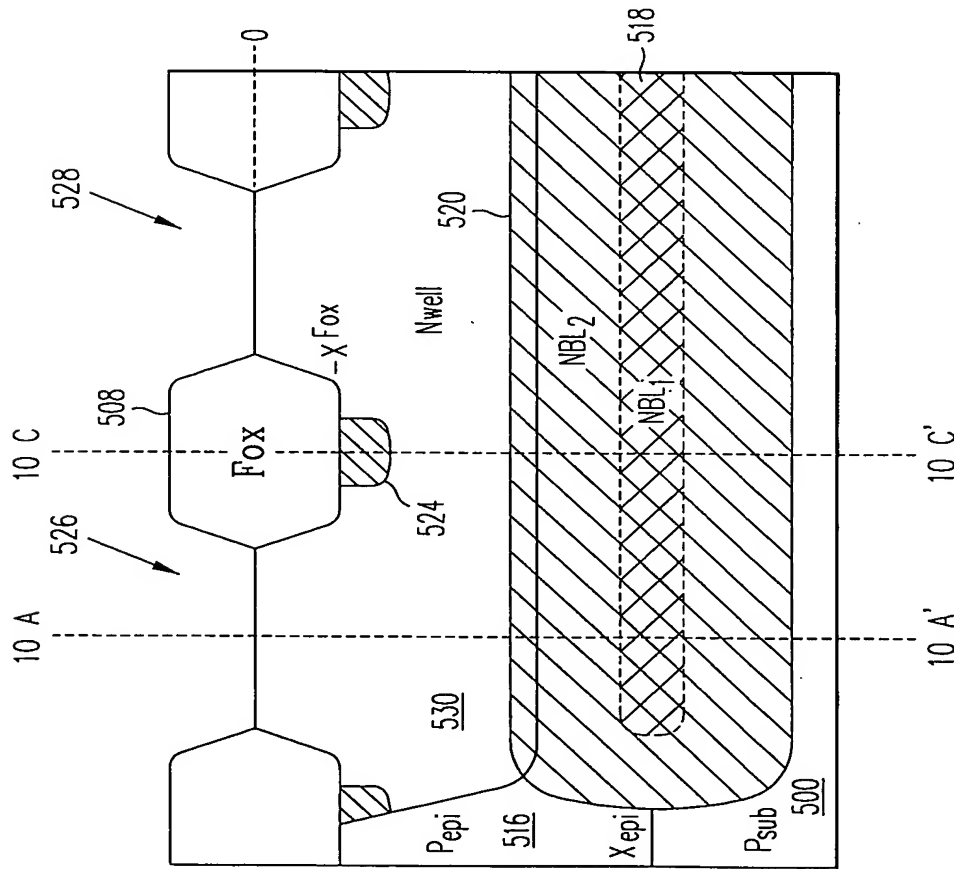


FIG. 10A  
(Prior Art)

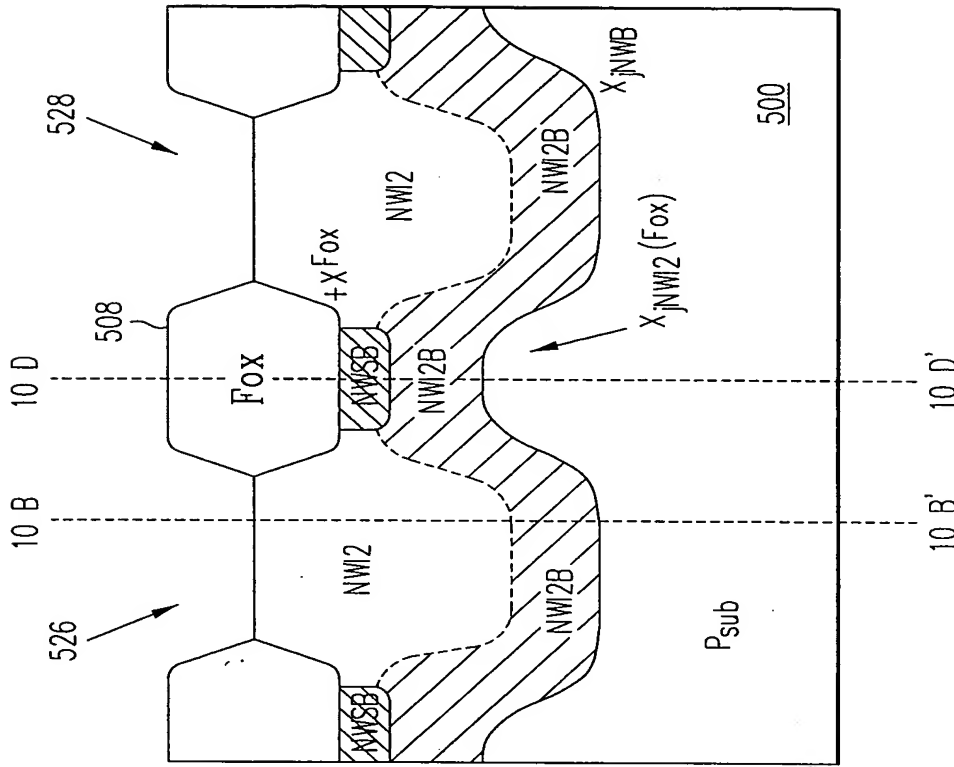


FIG. 10B

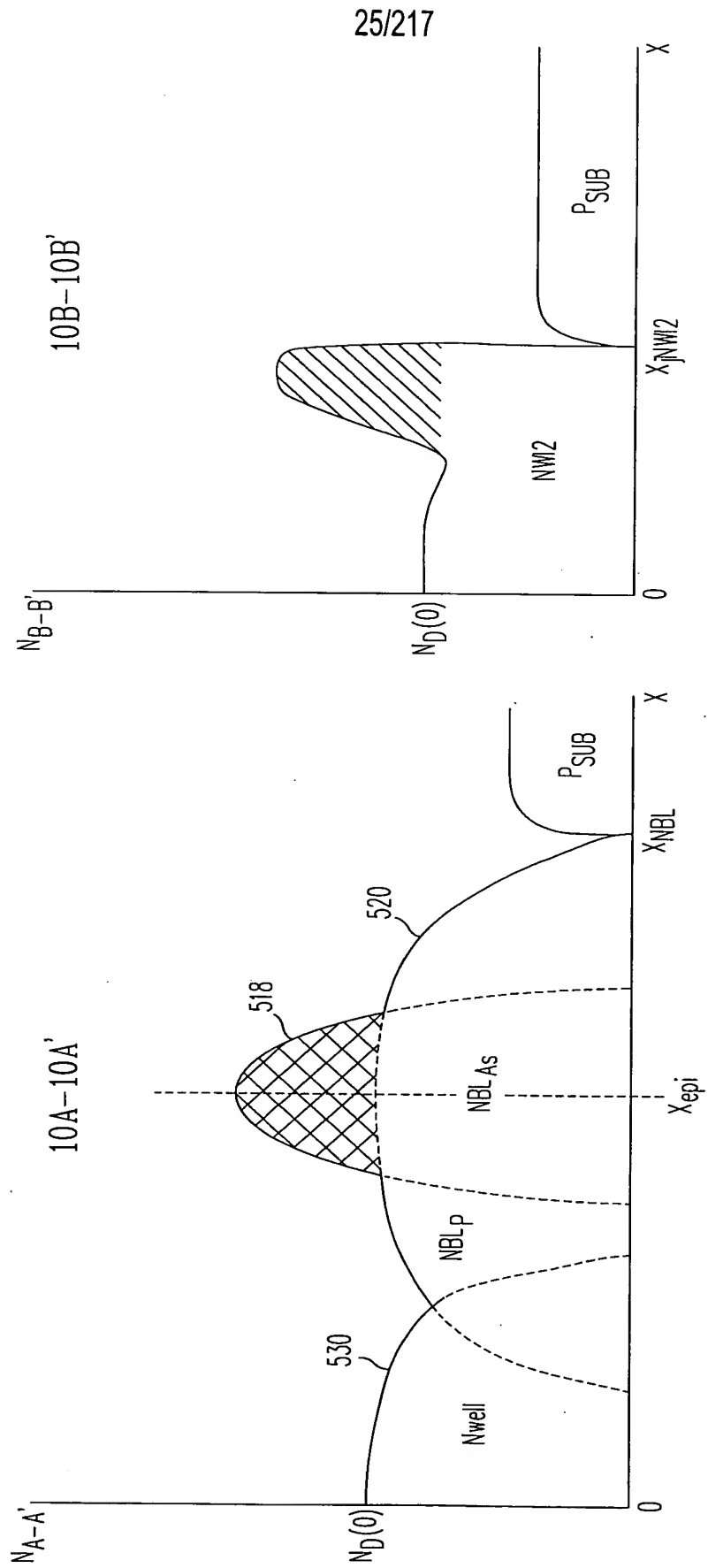


FIG. 10C  
(Prior Art)

FIG. 10D

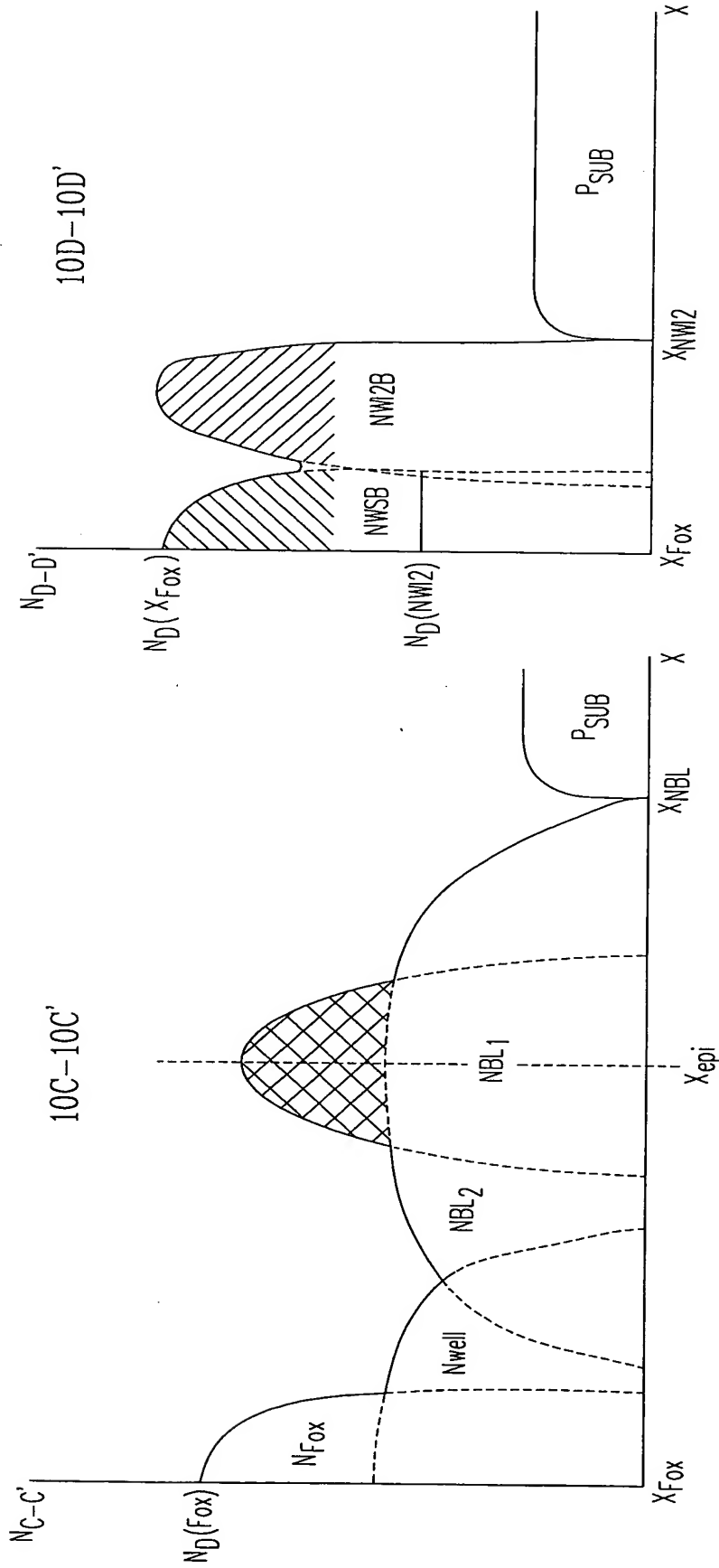
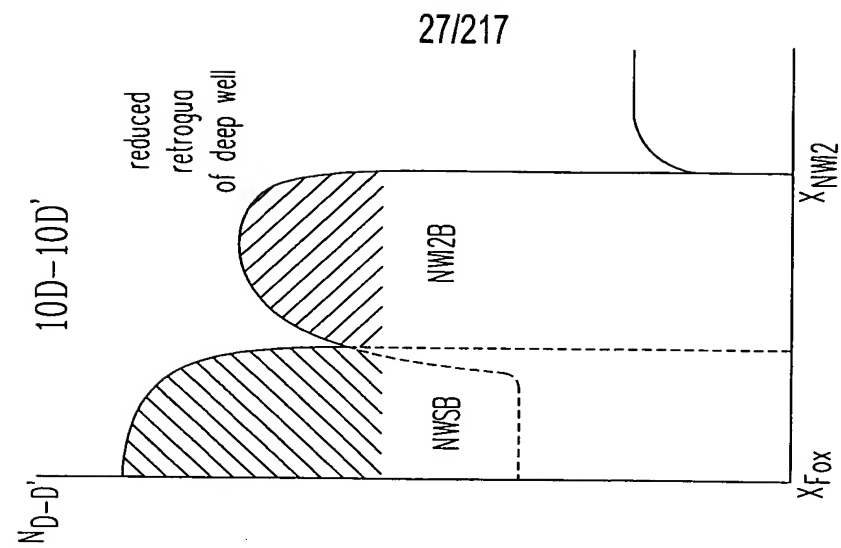
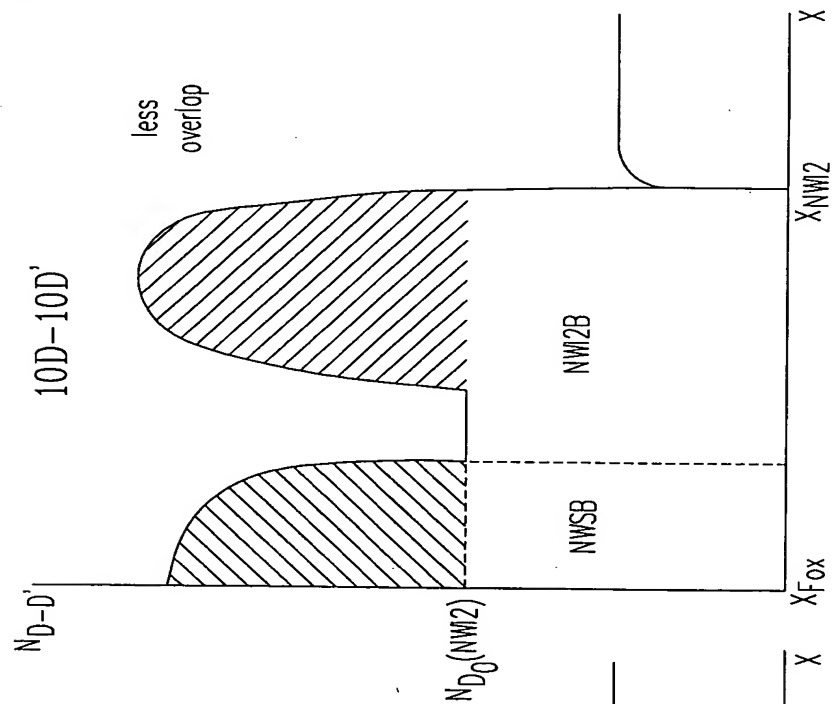
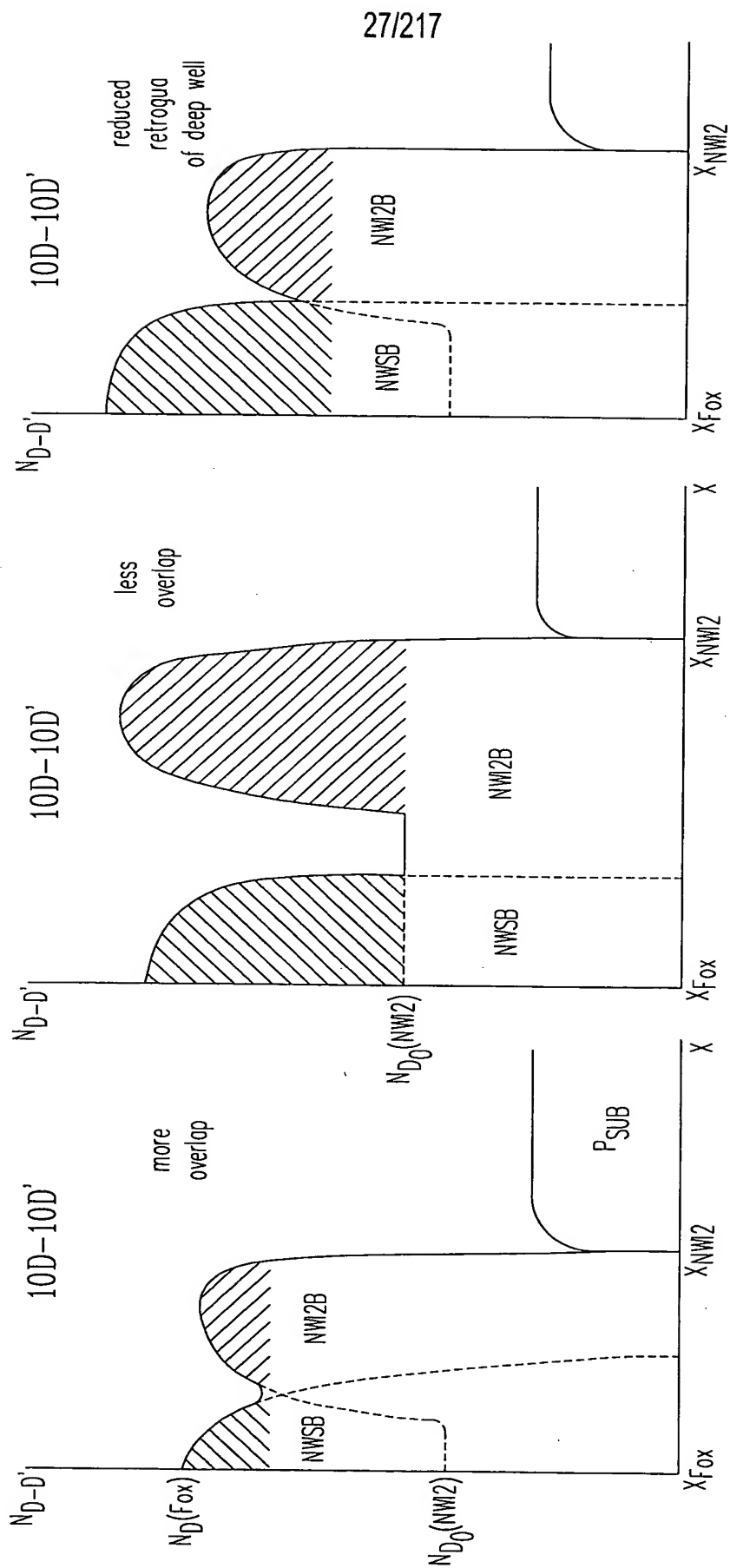


FIG. 10F

FIG. 10E  
(Prior Art)



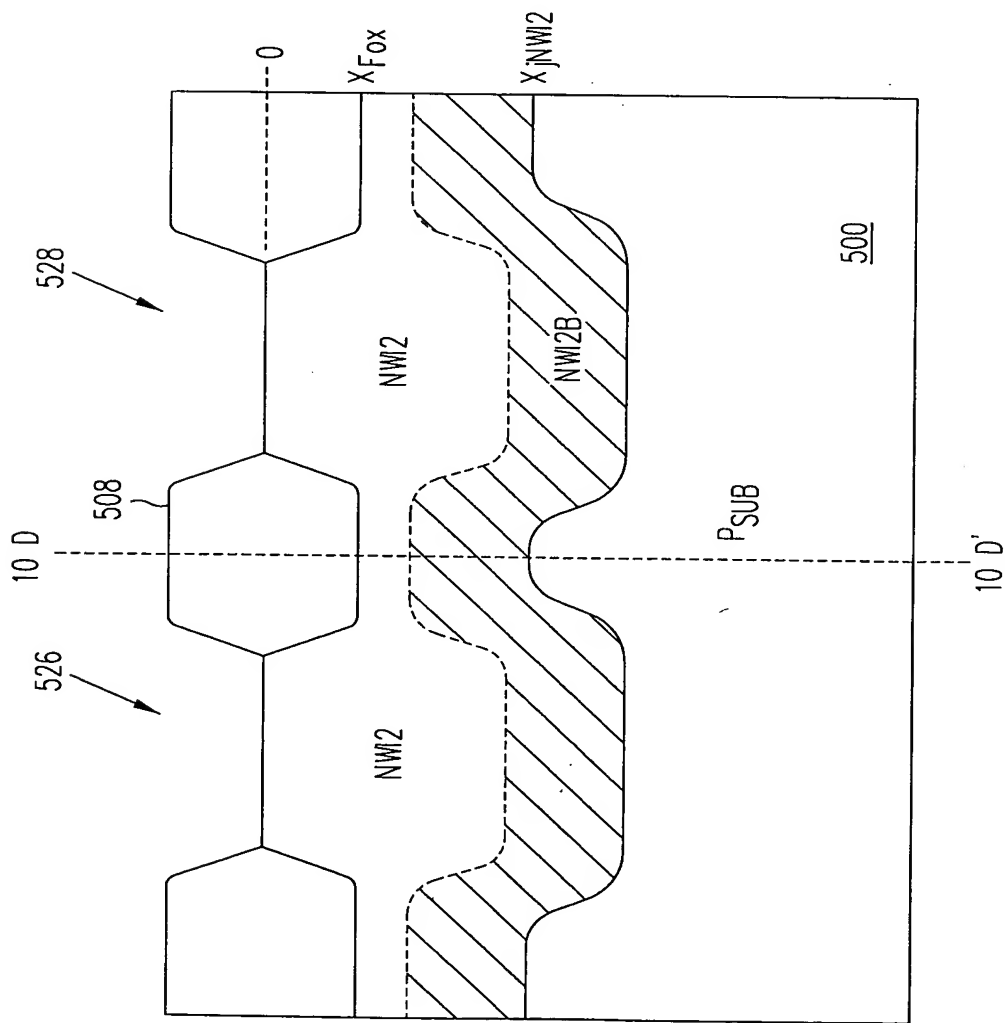


FIG. 10J

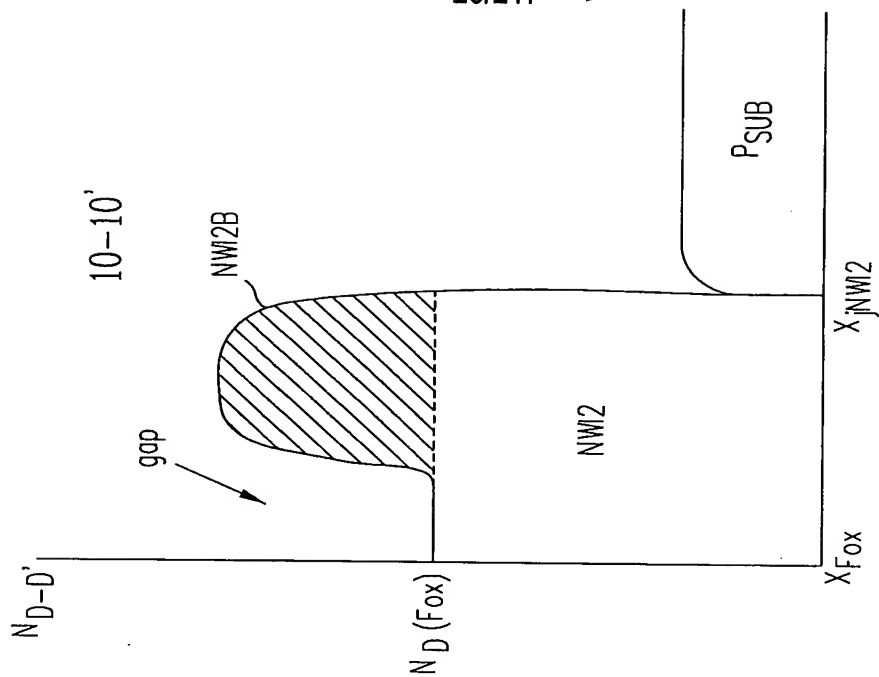


FIG. 10K



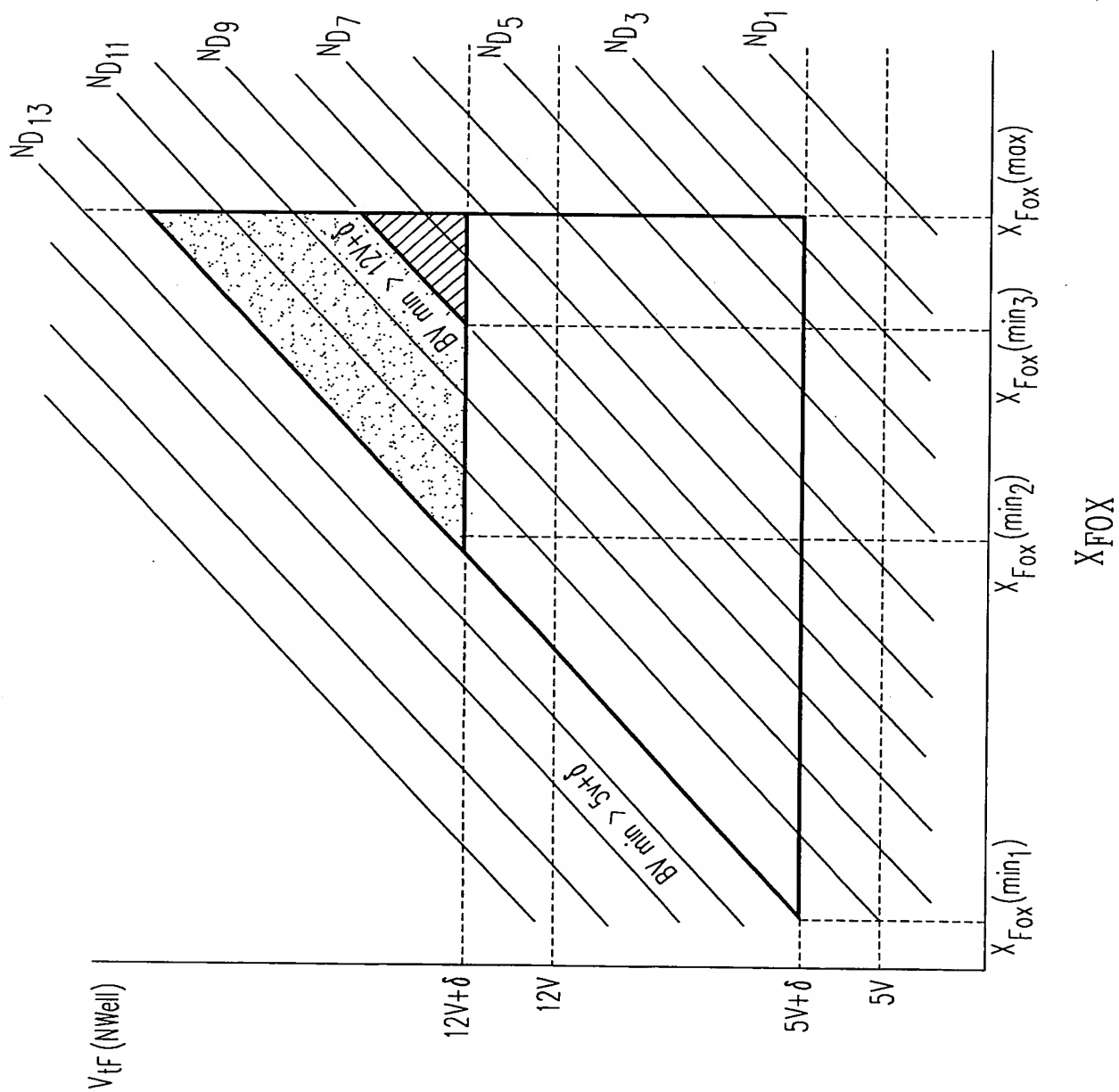


FIG. 10L

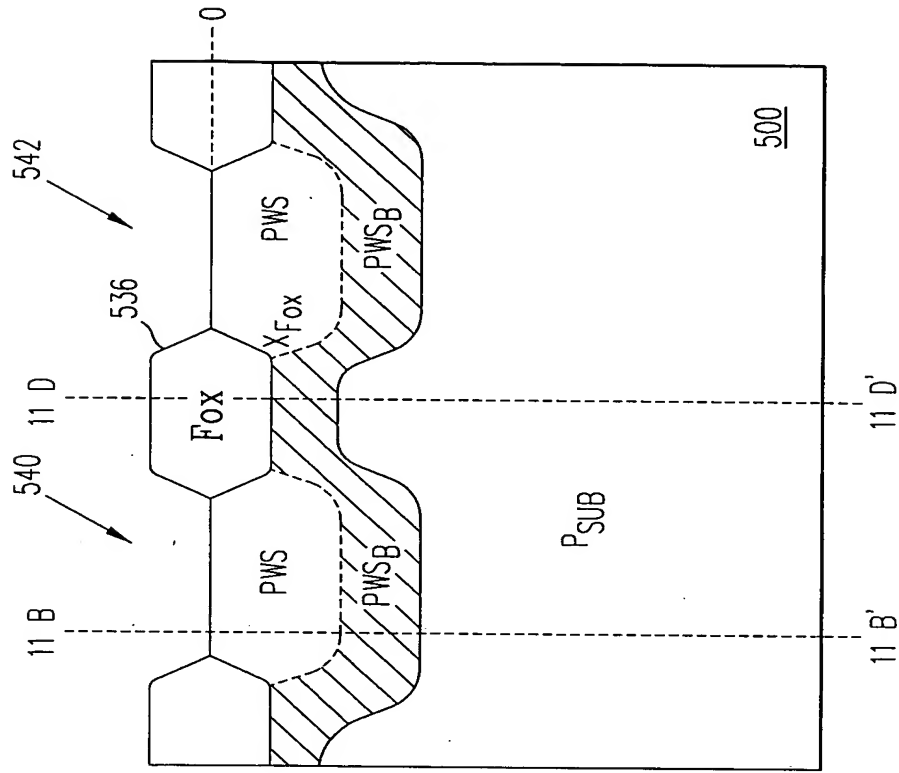
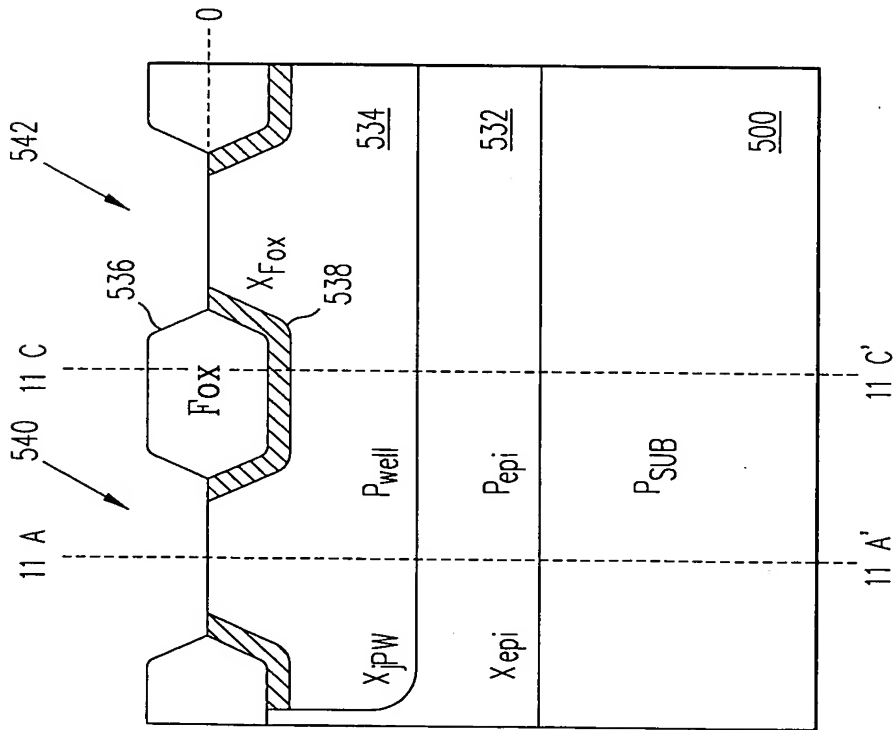


FIG. 11B



**FIG. 11A**

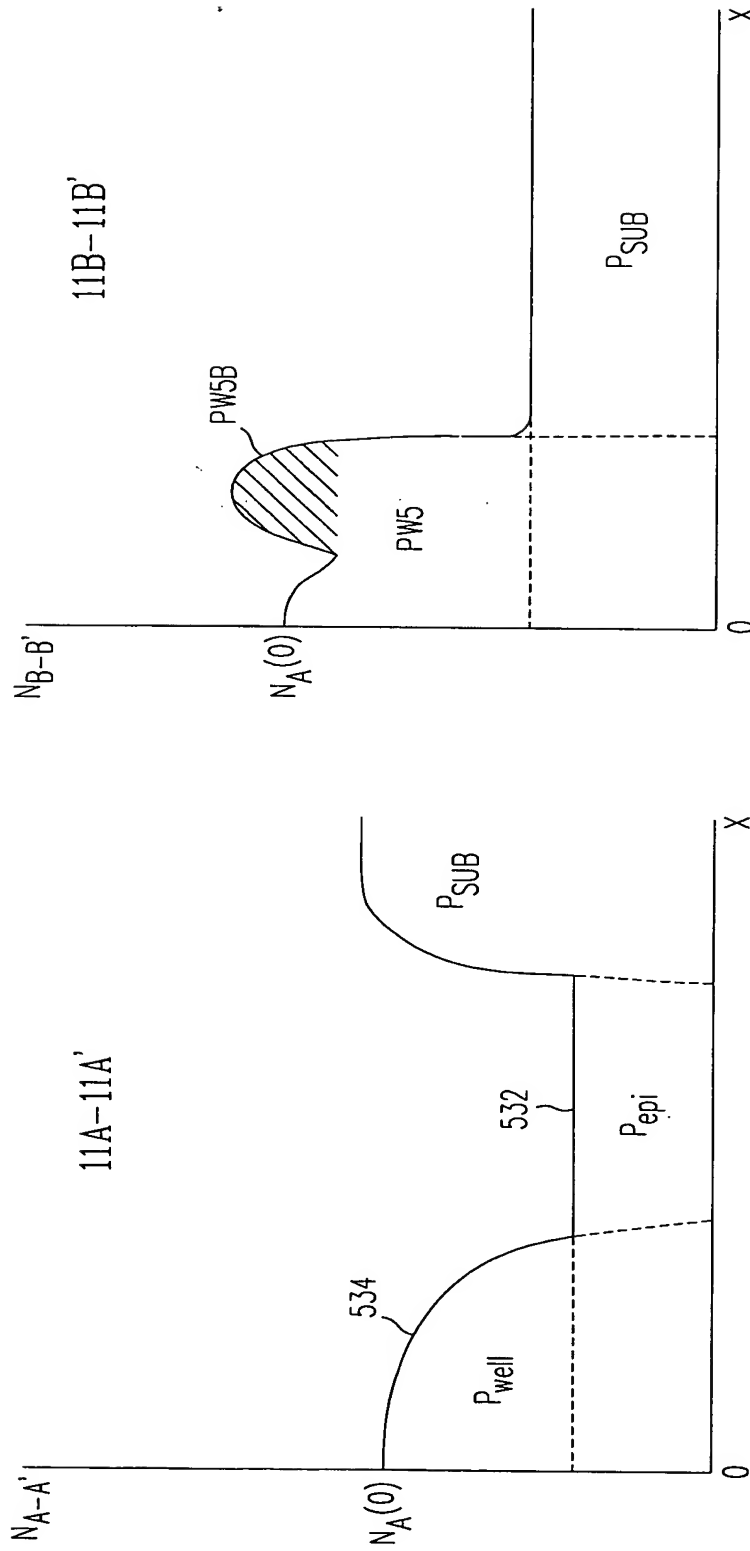


FIG. 11C

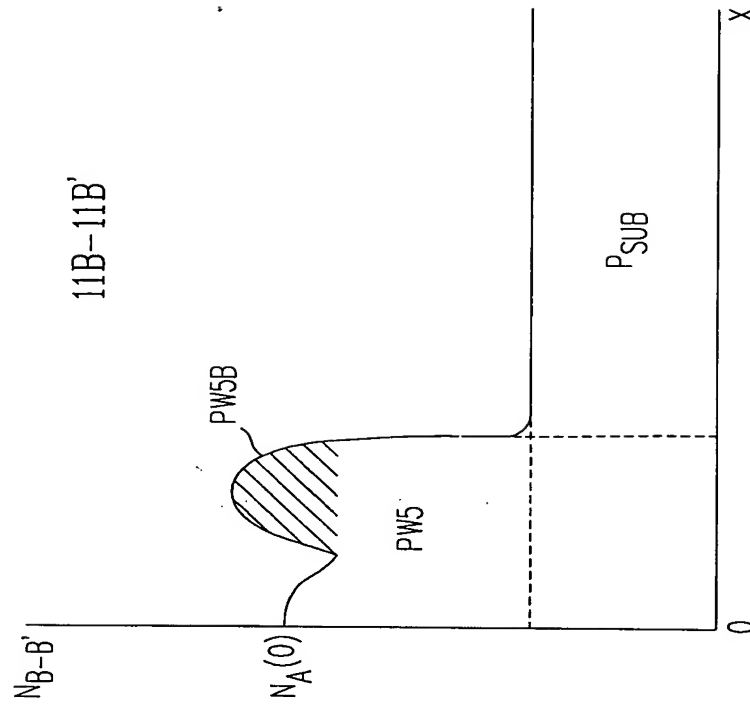


FIG. 11D

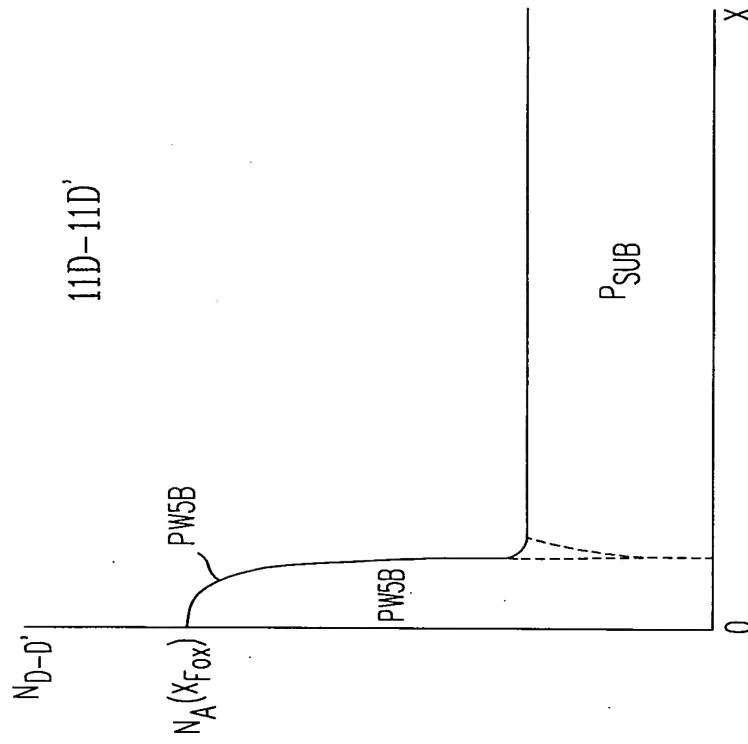


FIG. 11F

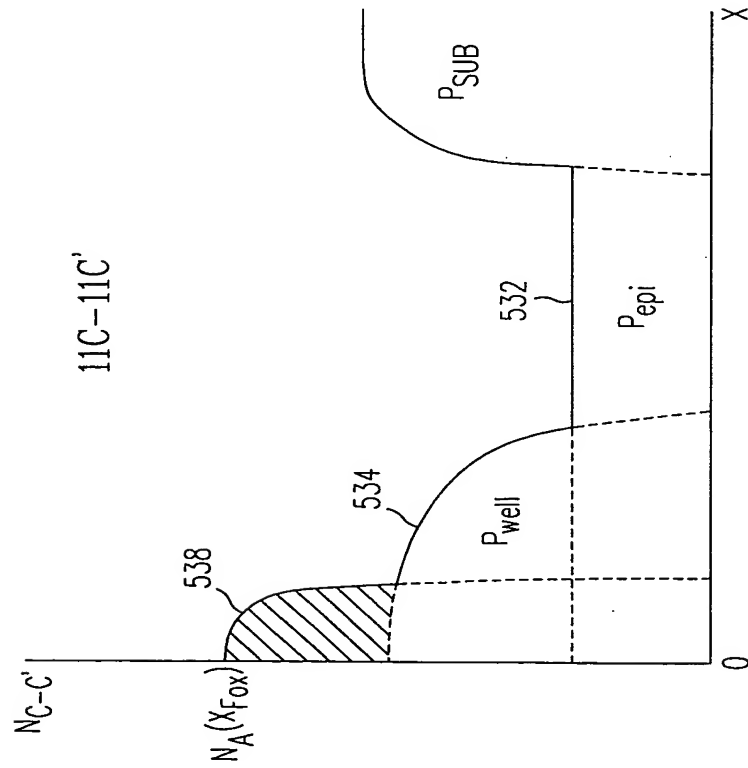


FIG. 11E

**FIG. 11G**

11E-11E'

$N_A(0)$

544

$P_{well}$

532

$P_{epi}$

$P_{SUB}$

0

X

FIG. 11I

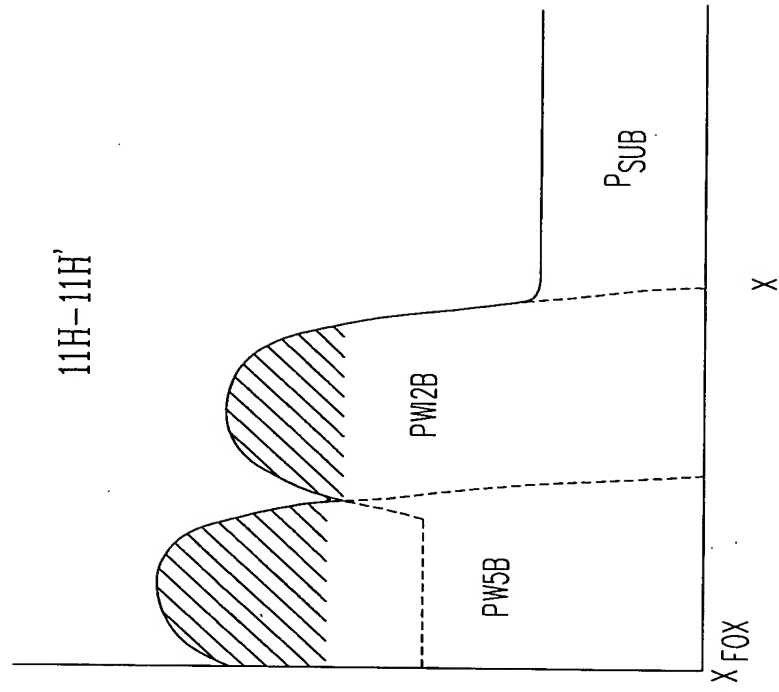


FIG. 11K

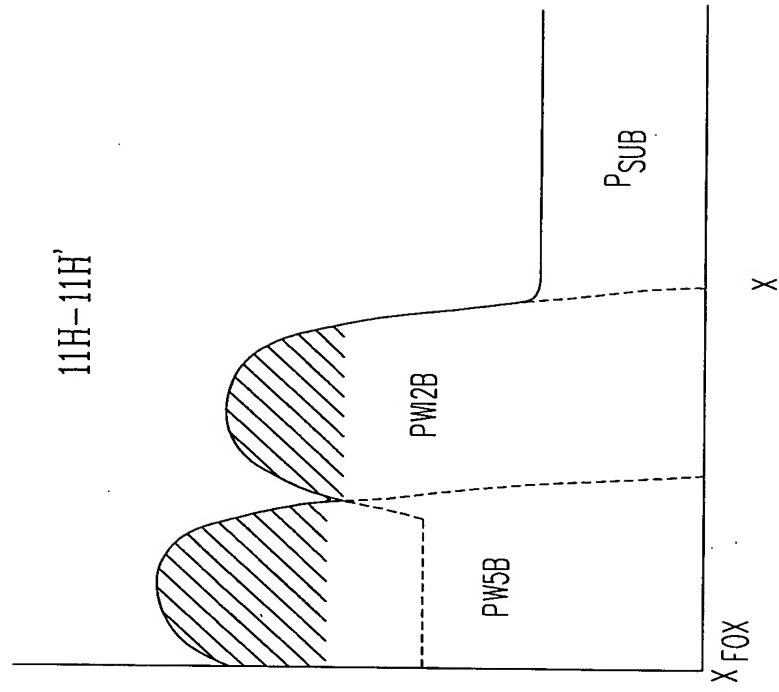


FIG. 11L

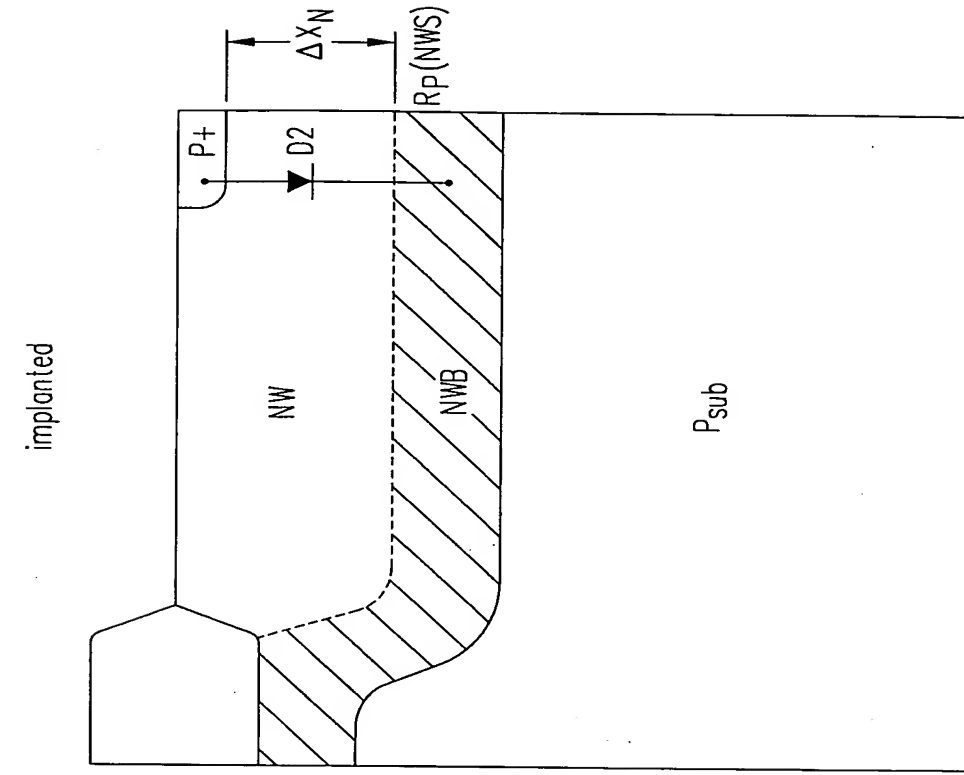


FIG. 12A

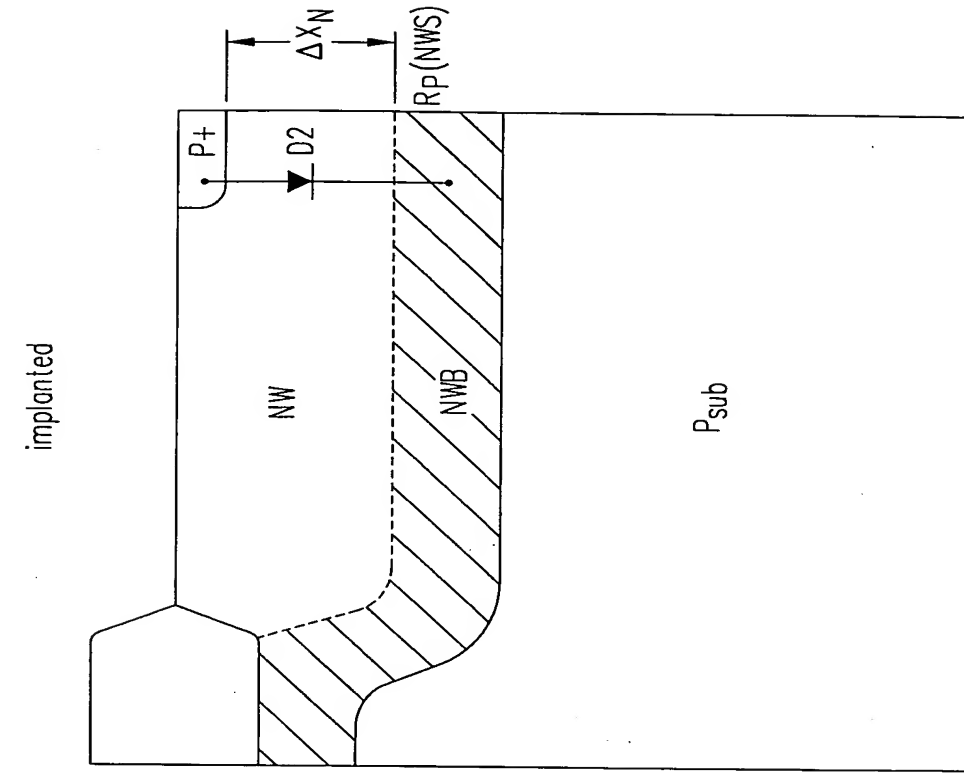


FIG. 12B



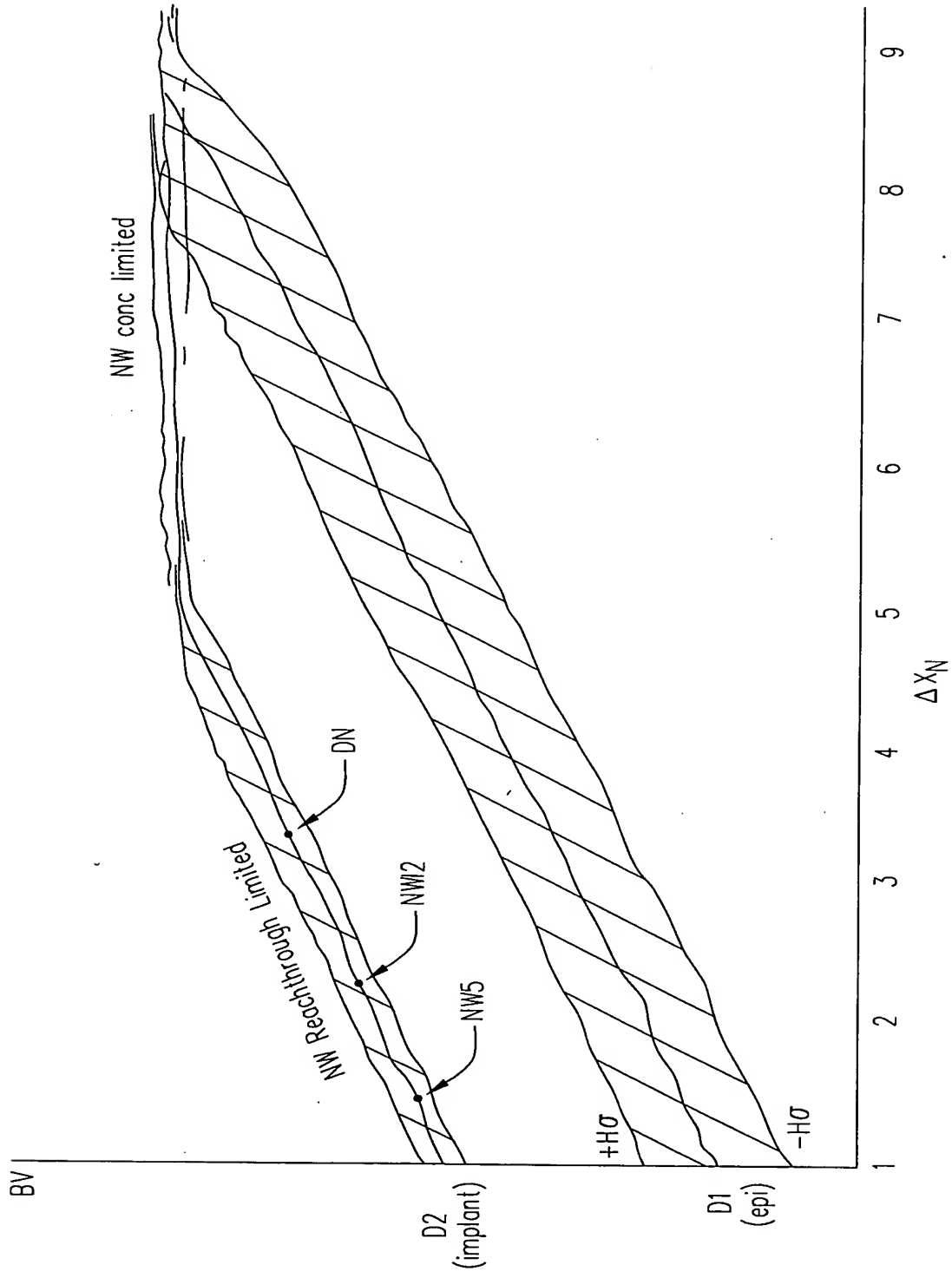


FIG. 12C

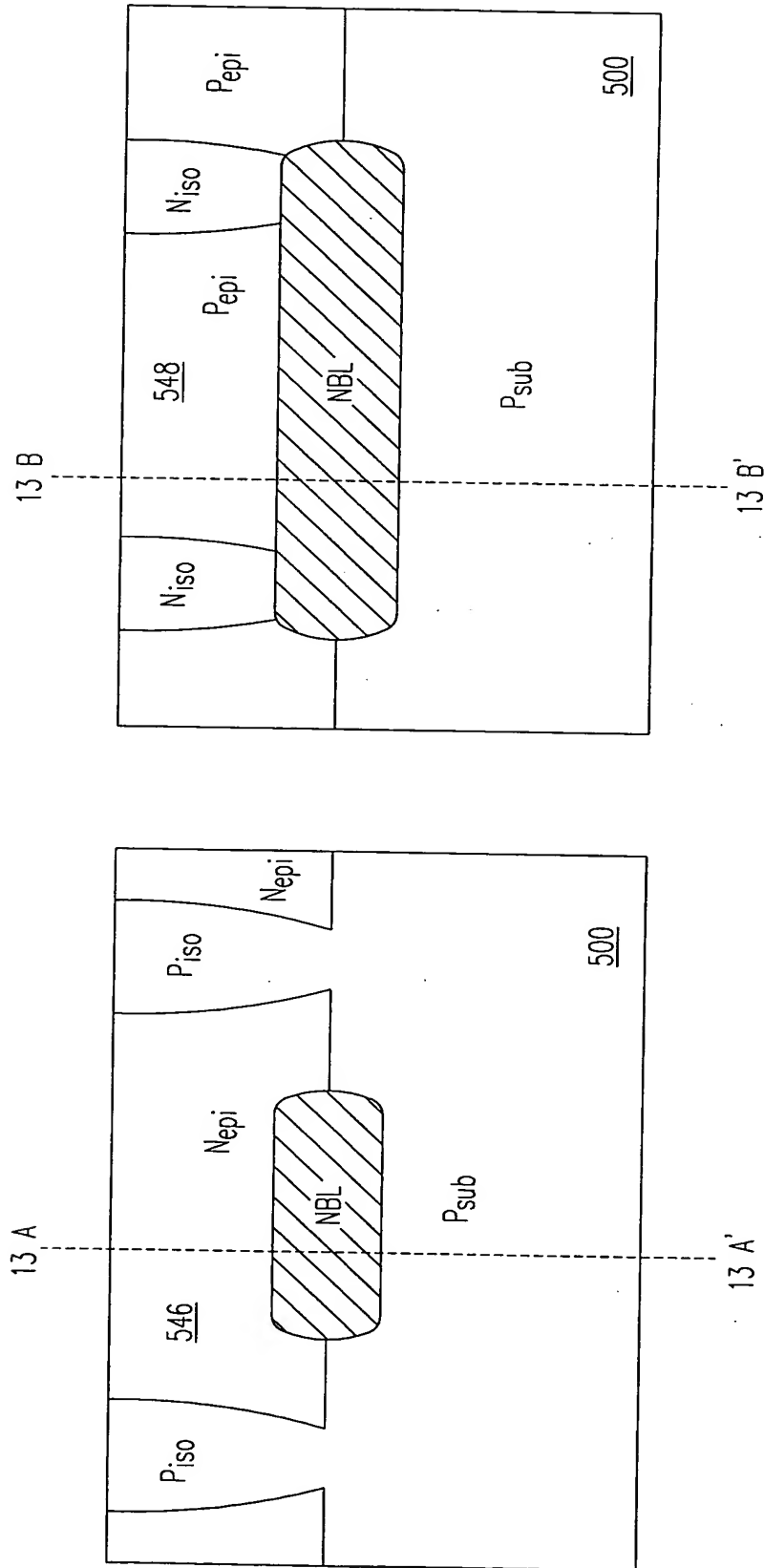


FIG. 13A  
(Prior Art)

FIG. 13B  
(Prior Art)

13B-13B'

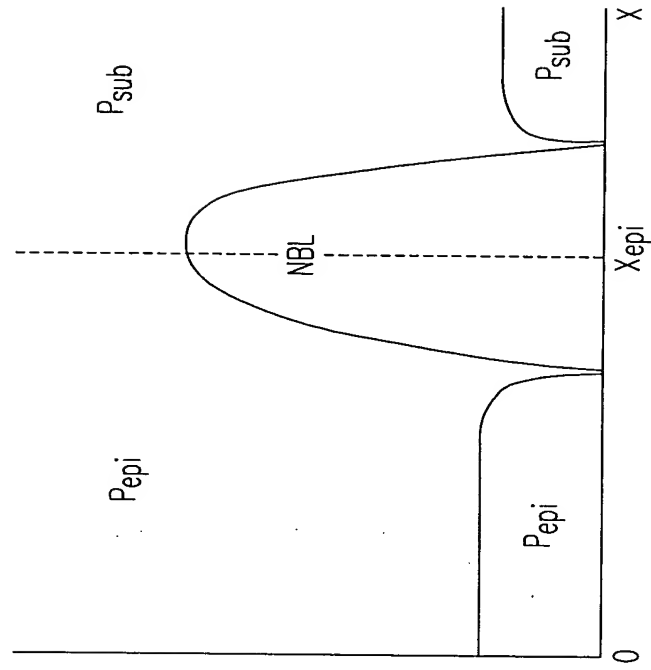


FIG. 13D

13A-13A'

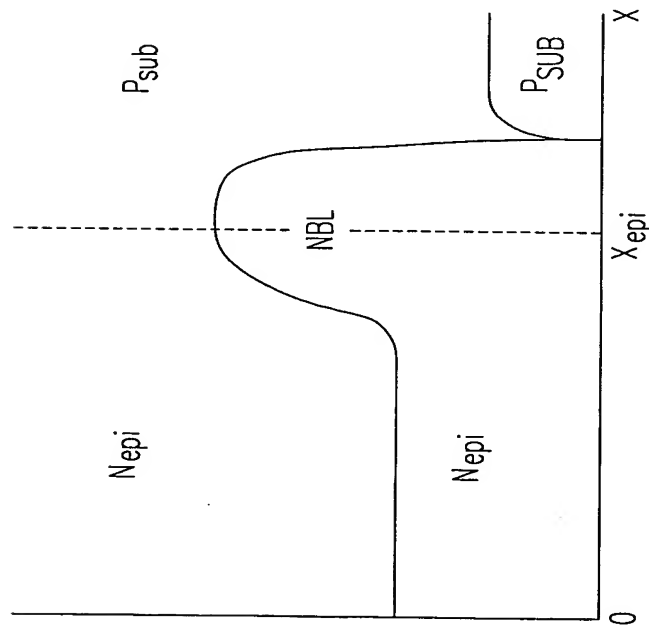


FIG. 13C

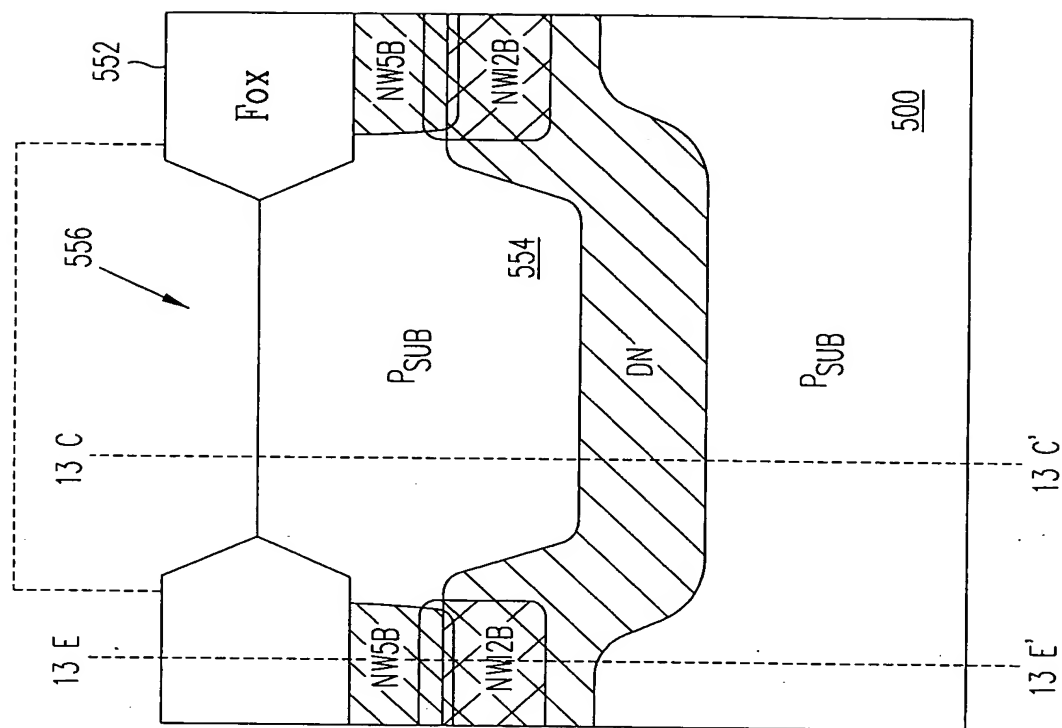


FIG. 13F

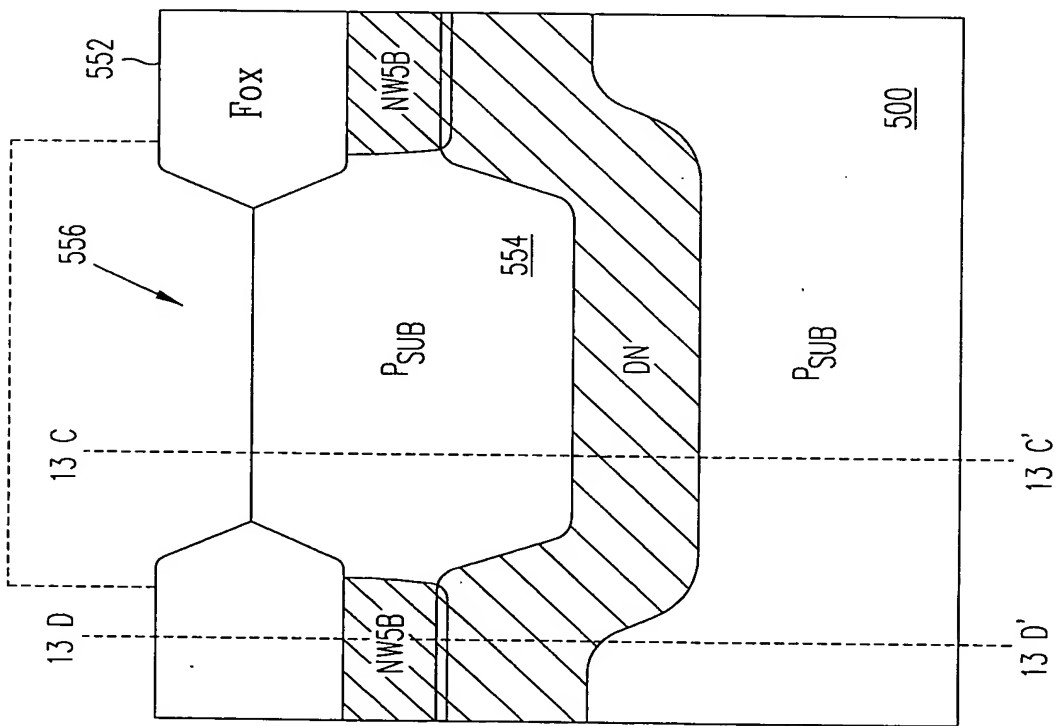


FIG. 13E

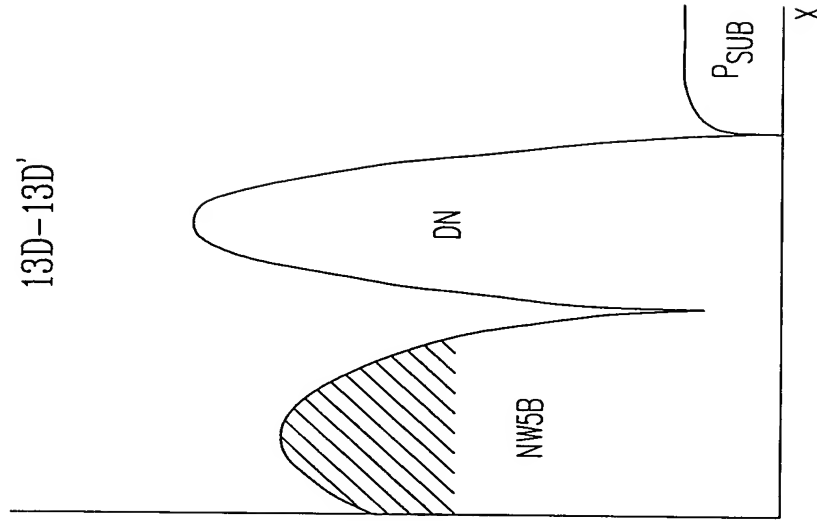


FIG. 13H

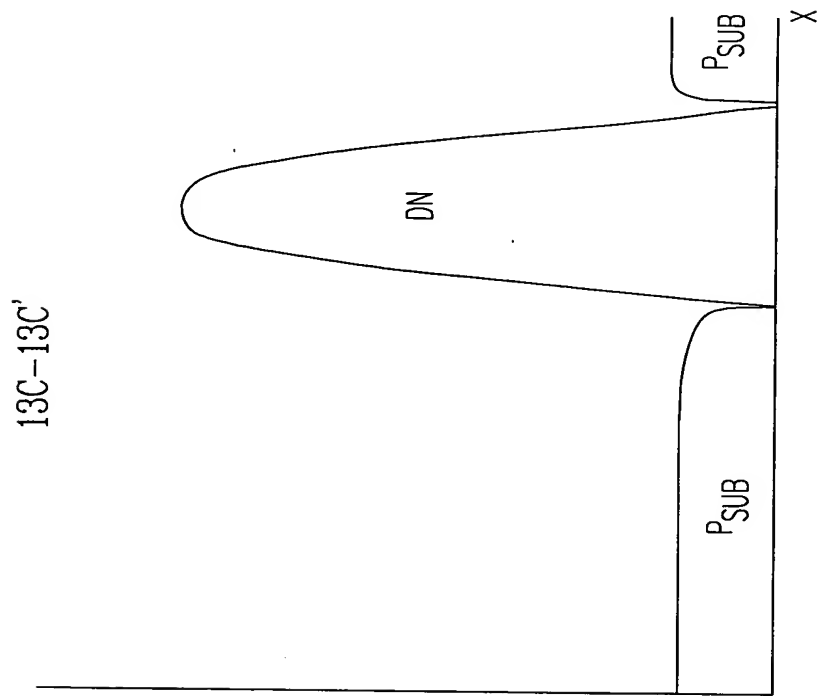


FIG. 13G

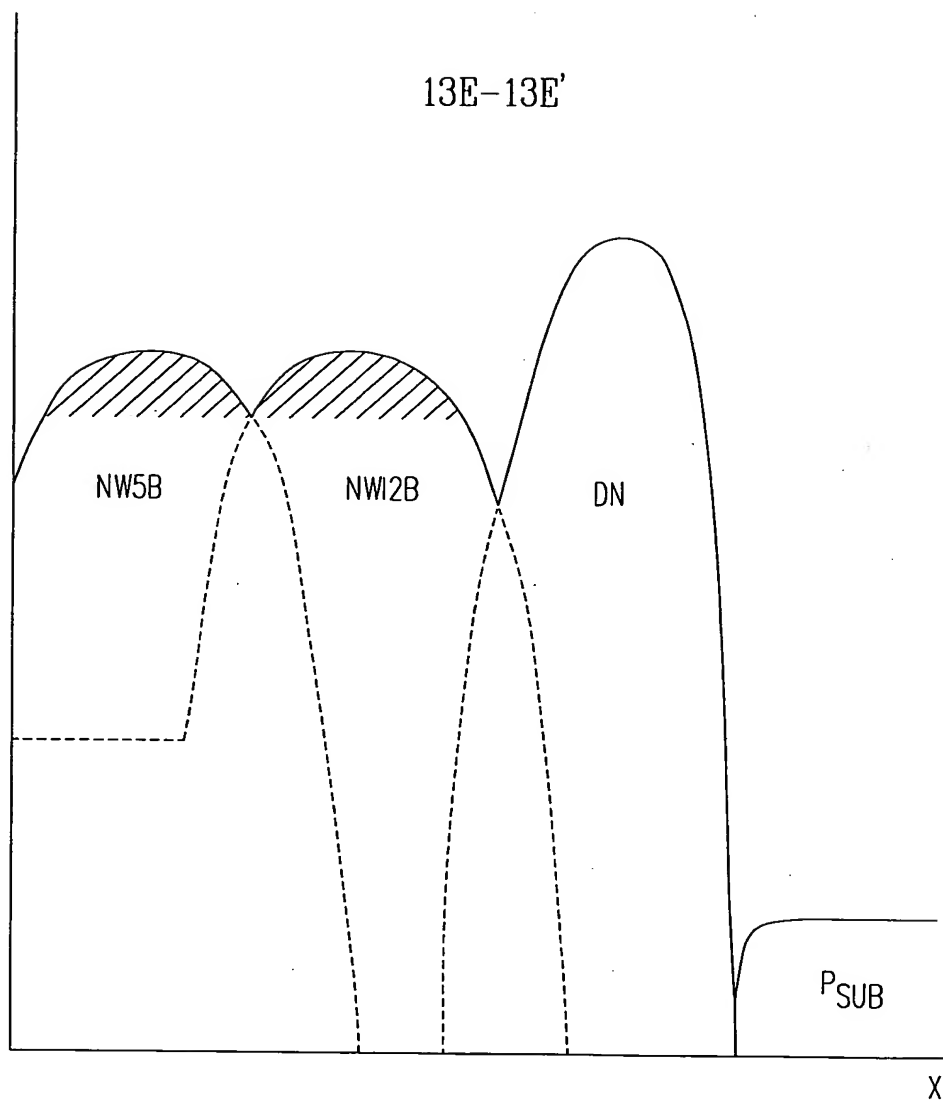


FIG. 13I

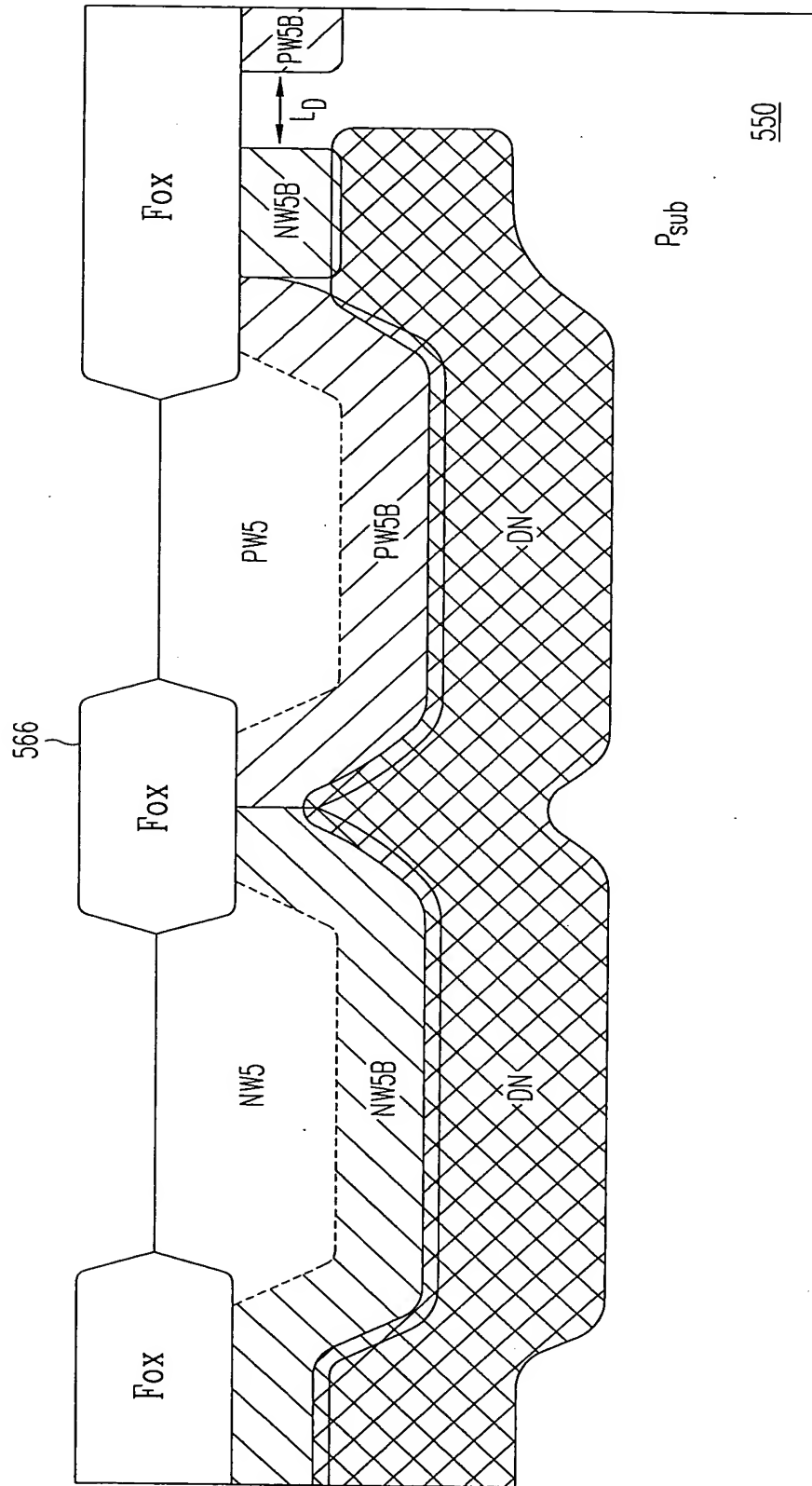


FIG. 14A

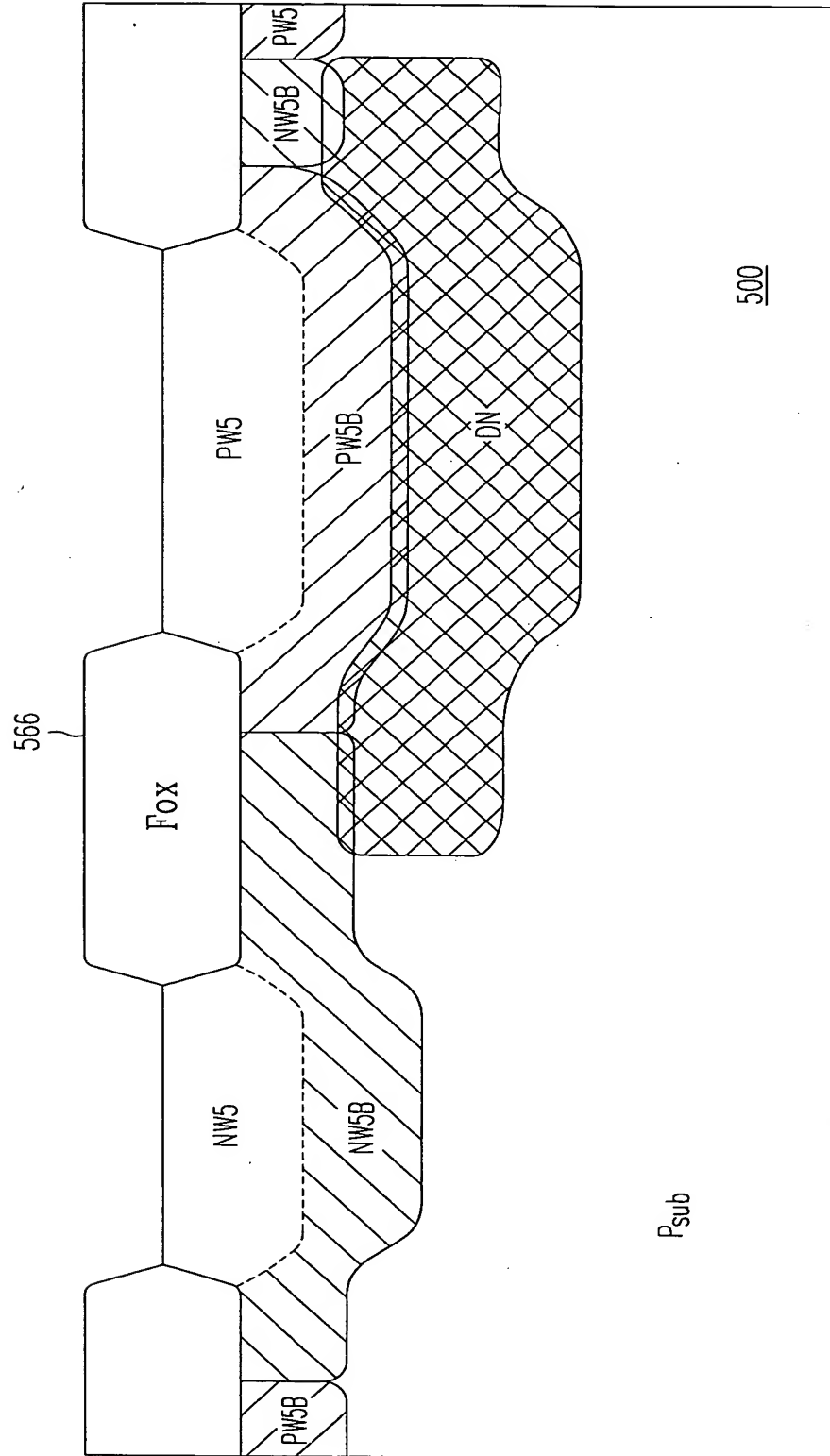


FIG. 14B



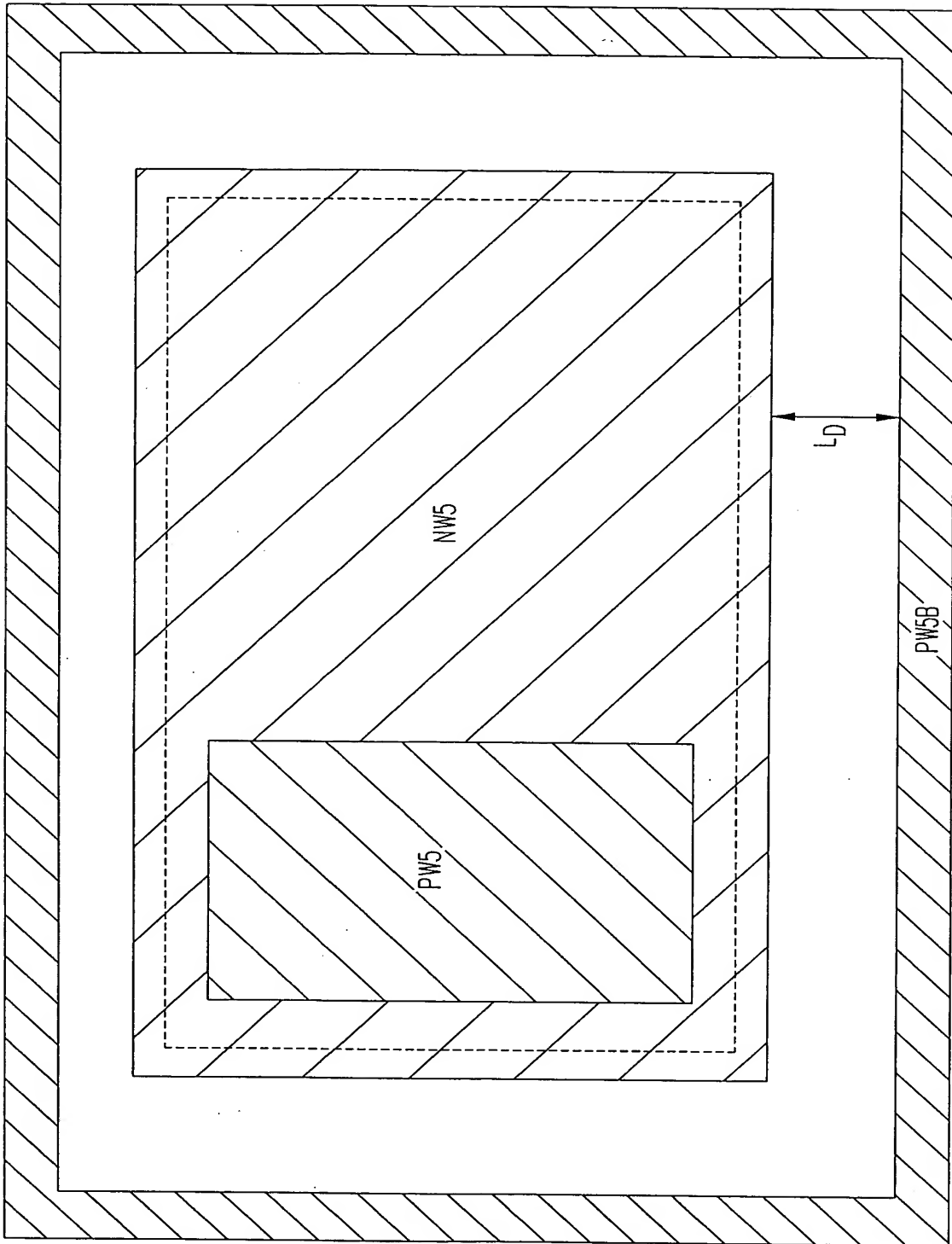


FIG. 14C

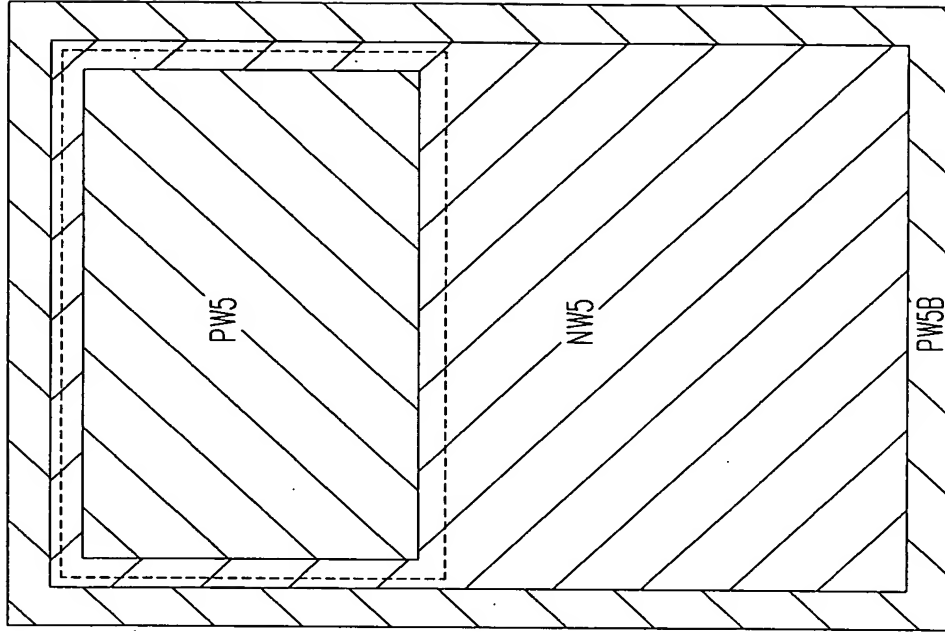


FIG. 14E

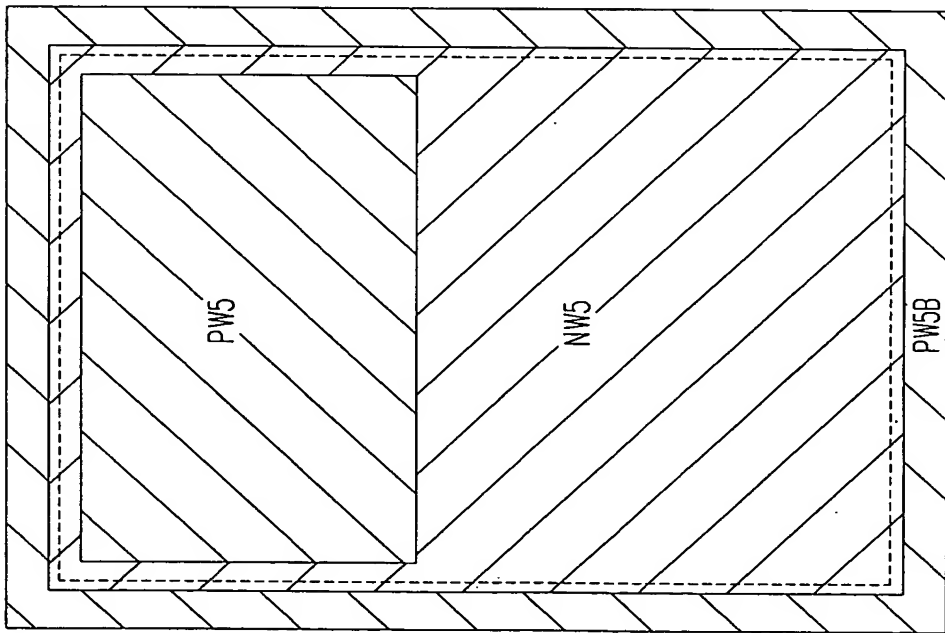


FIG. 14D

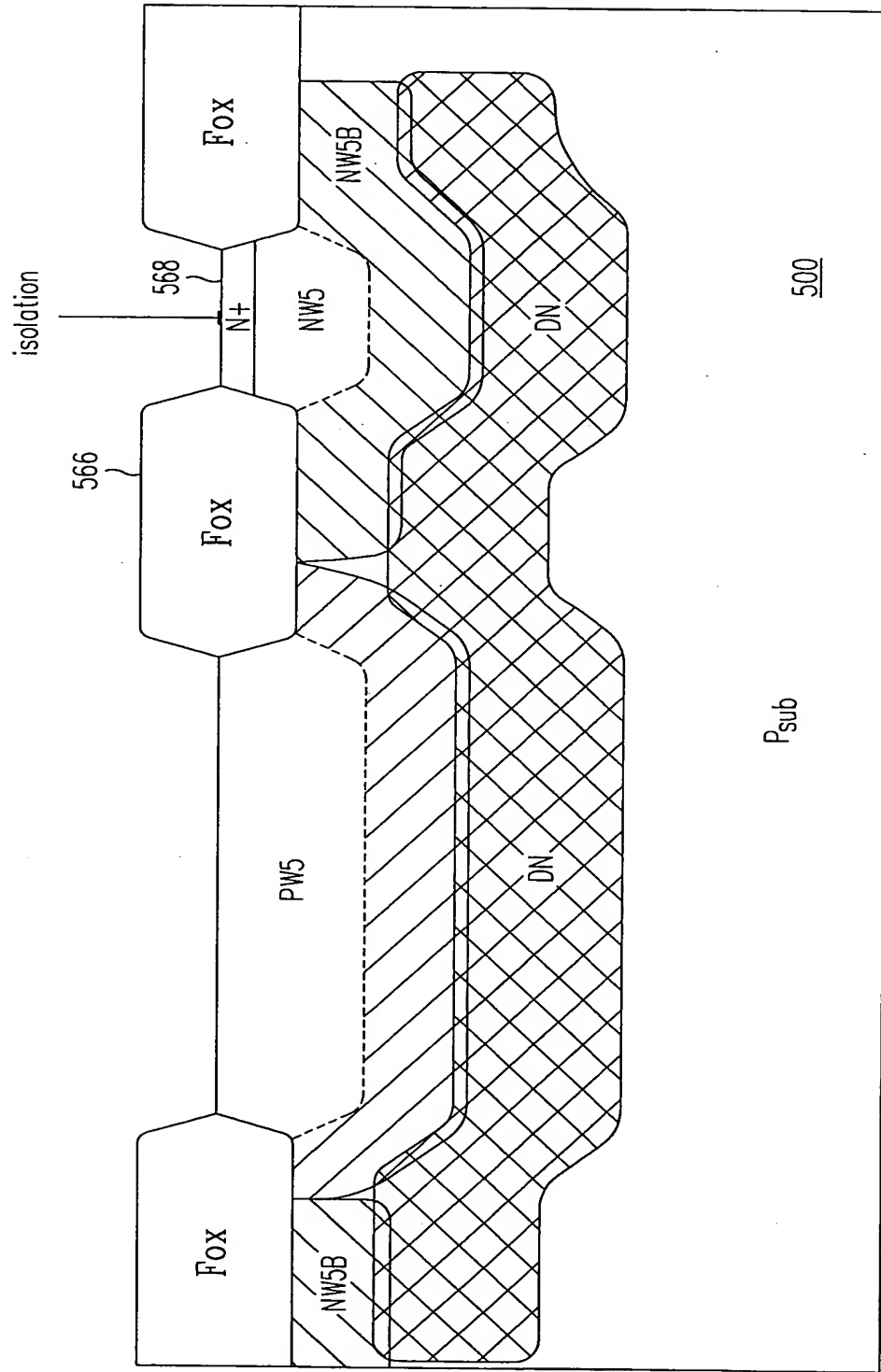


FIG. 14F

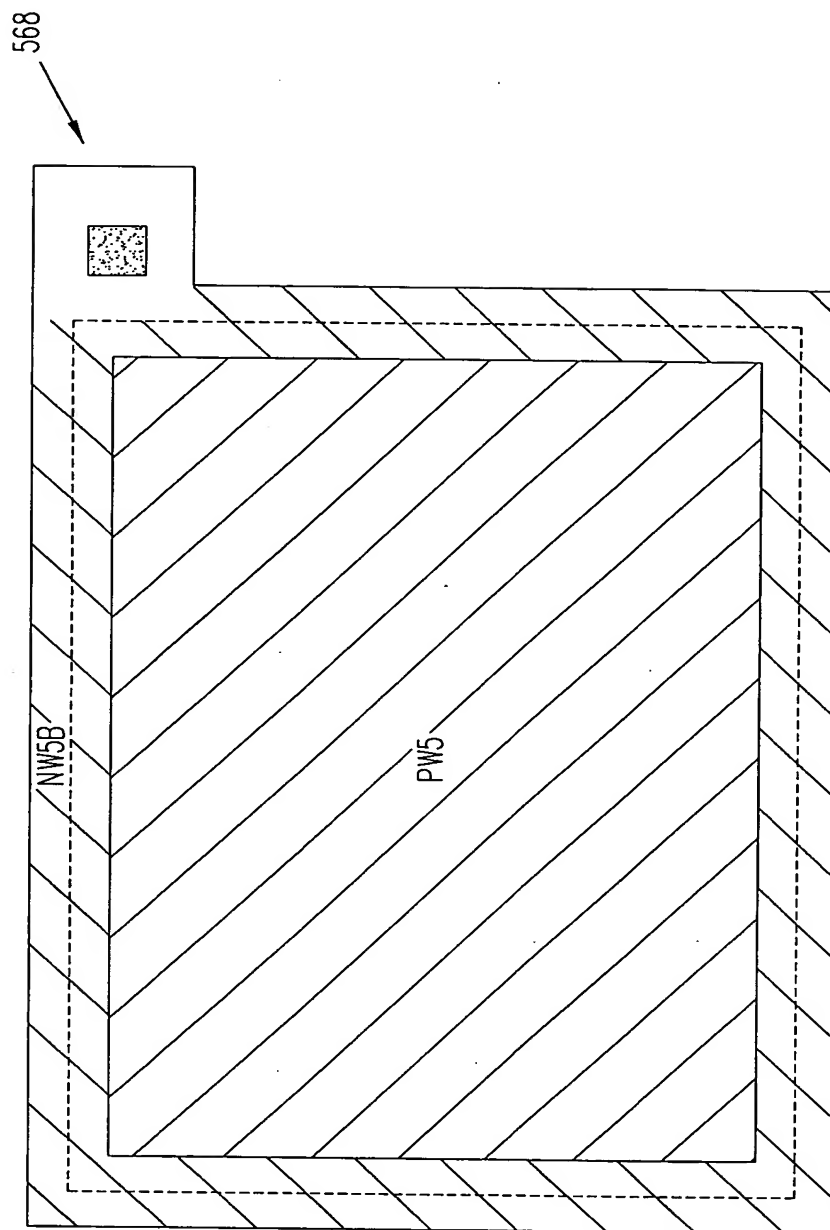


FIG. 14C

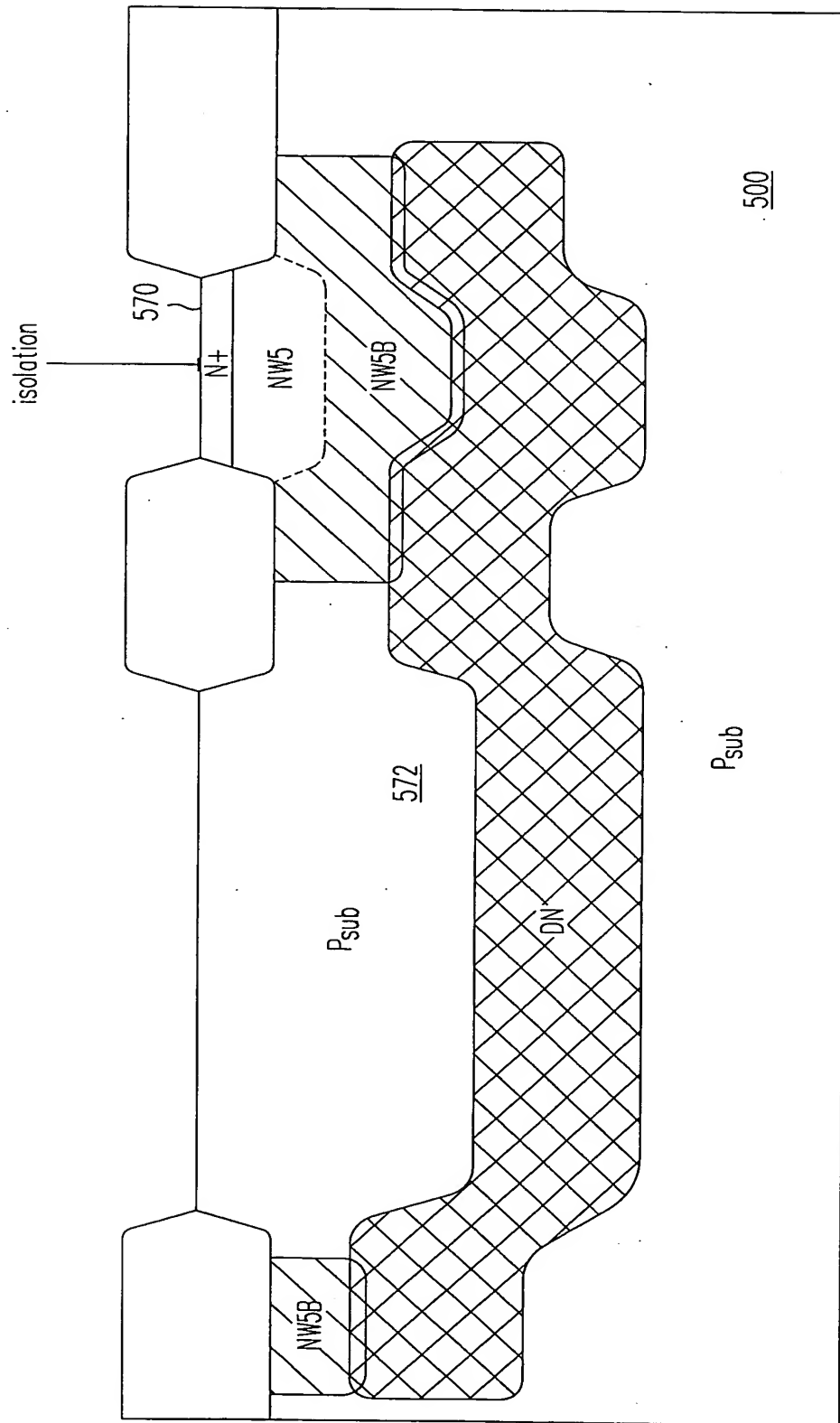


FIG. 14H

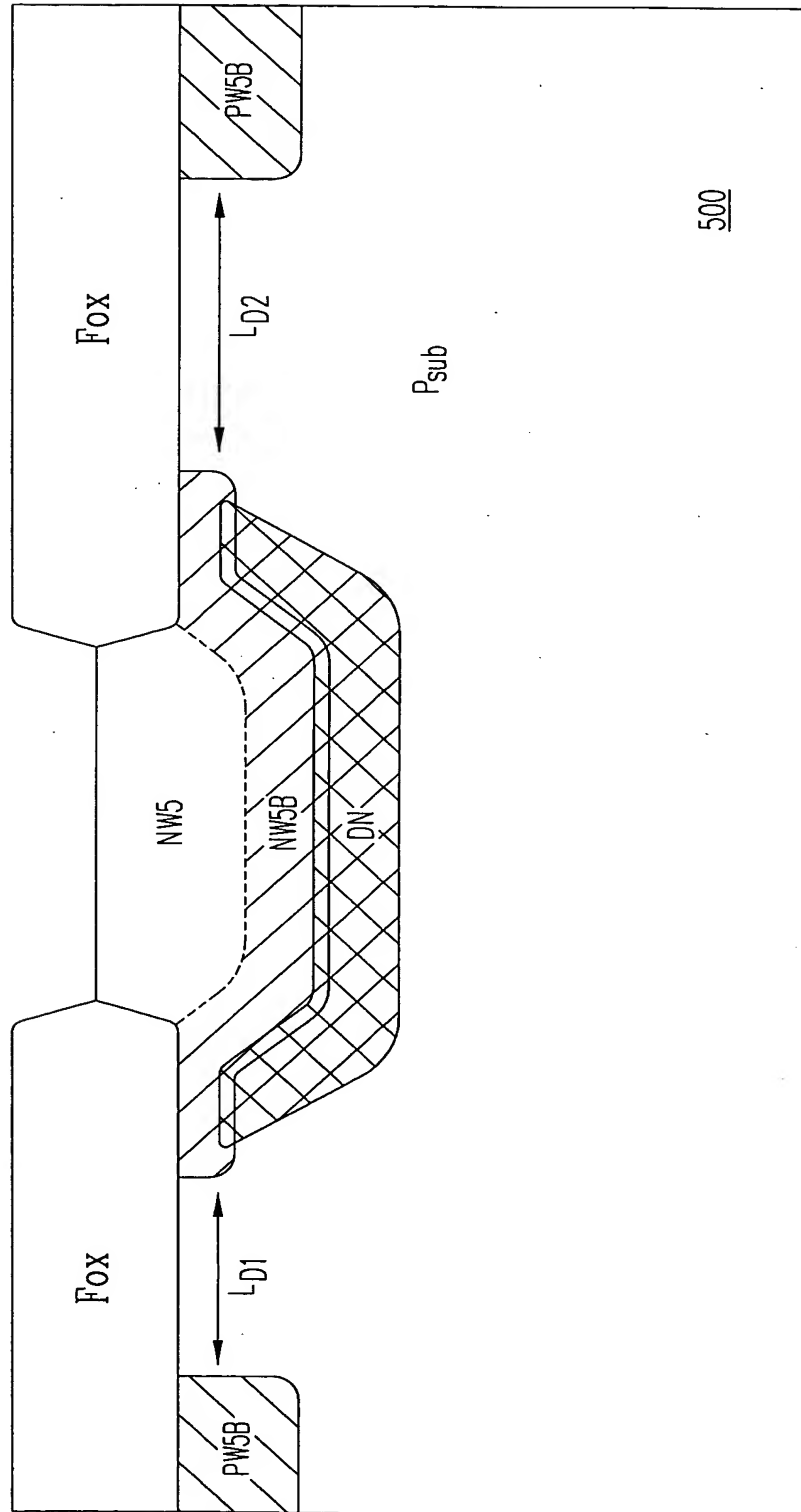


FIG. 14I

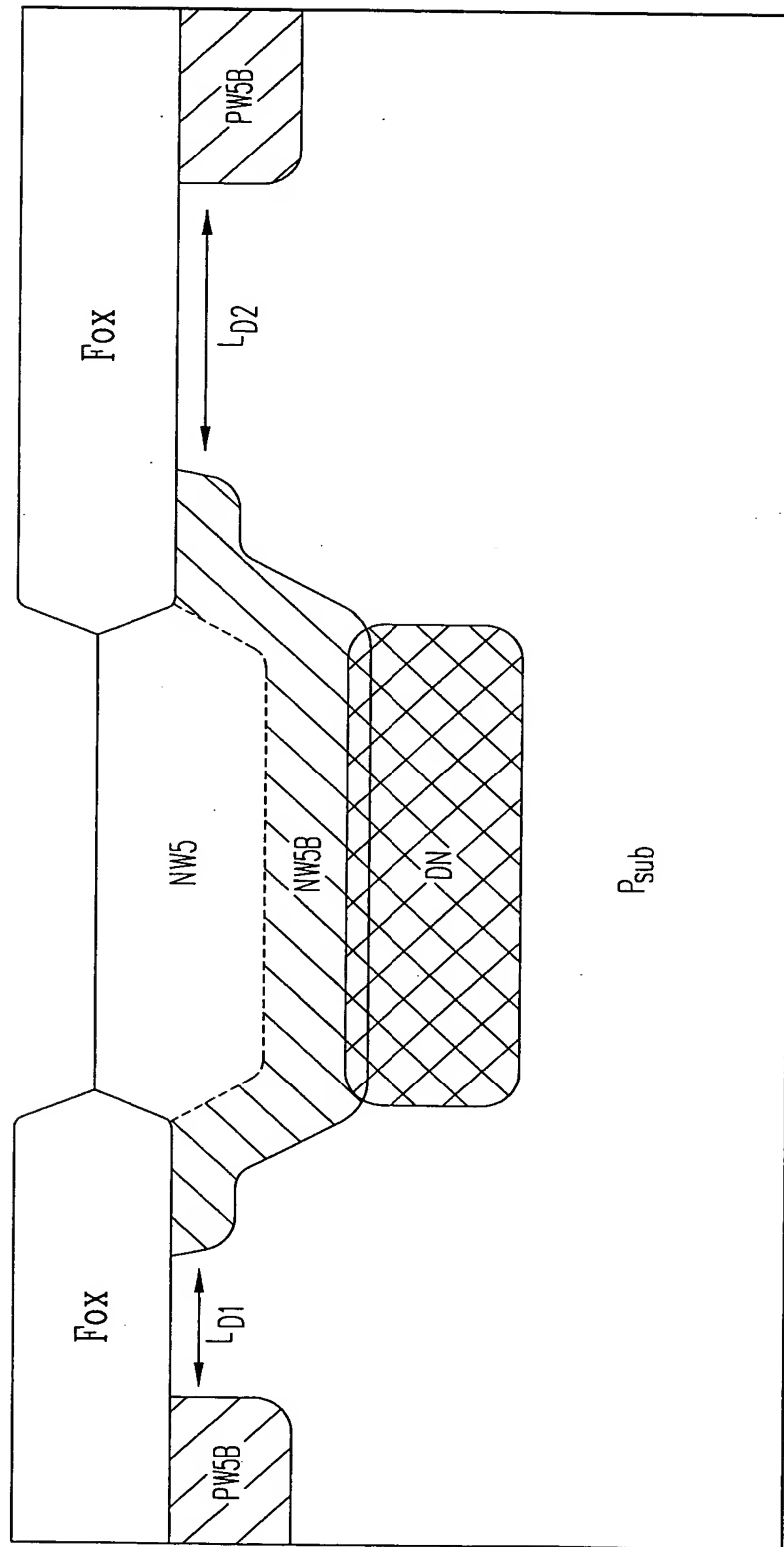


FIG. 14J

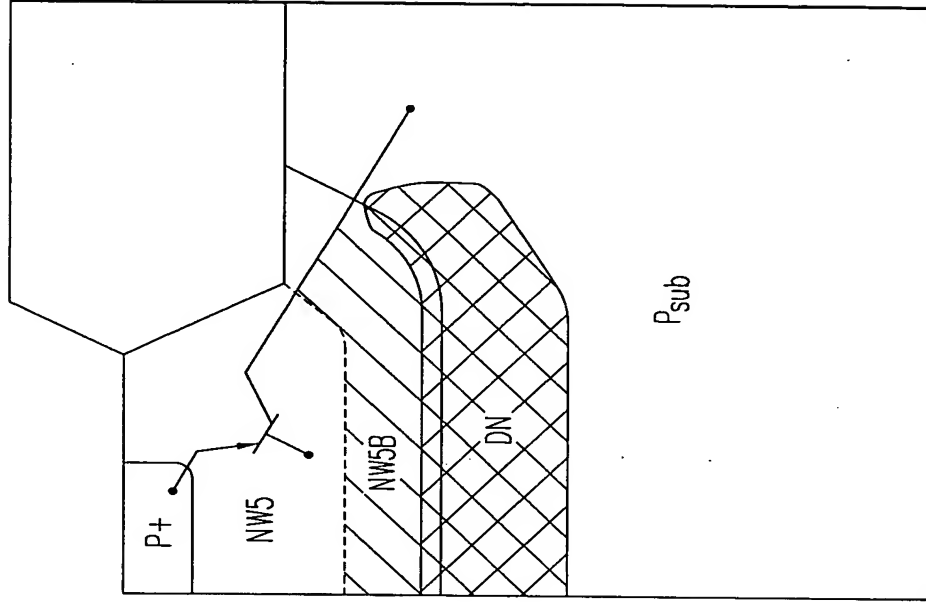


FIG. 14L

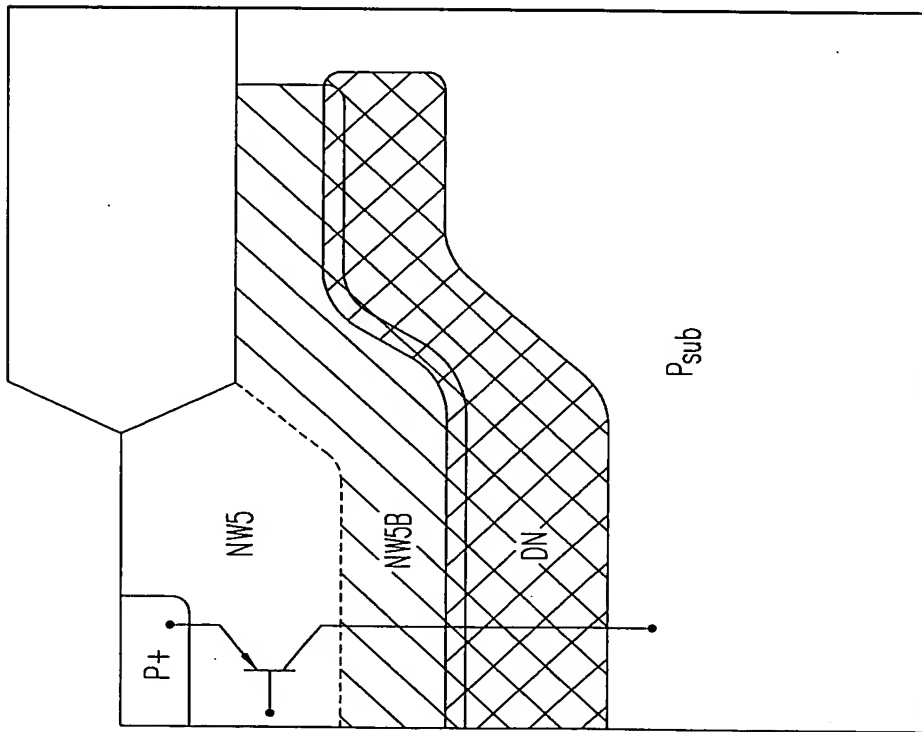


FIG. 14K



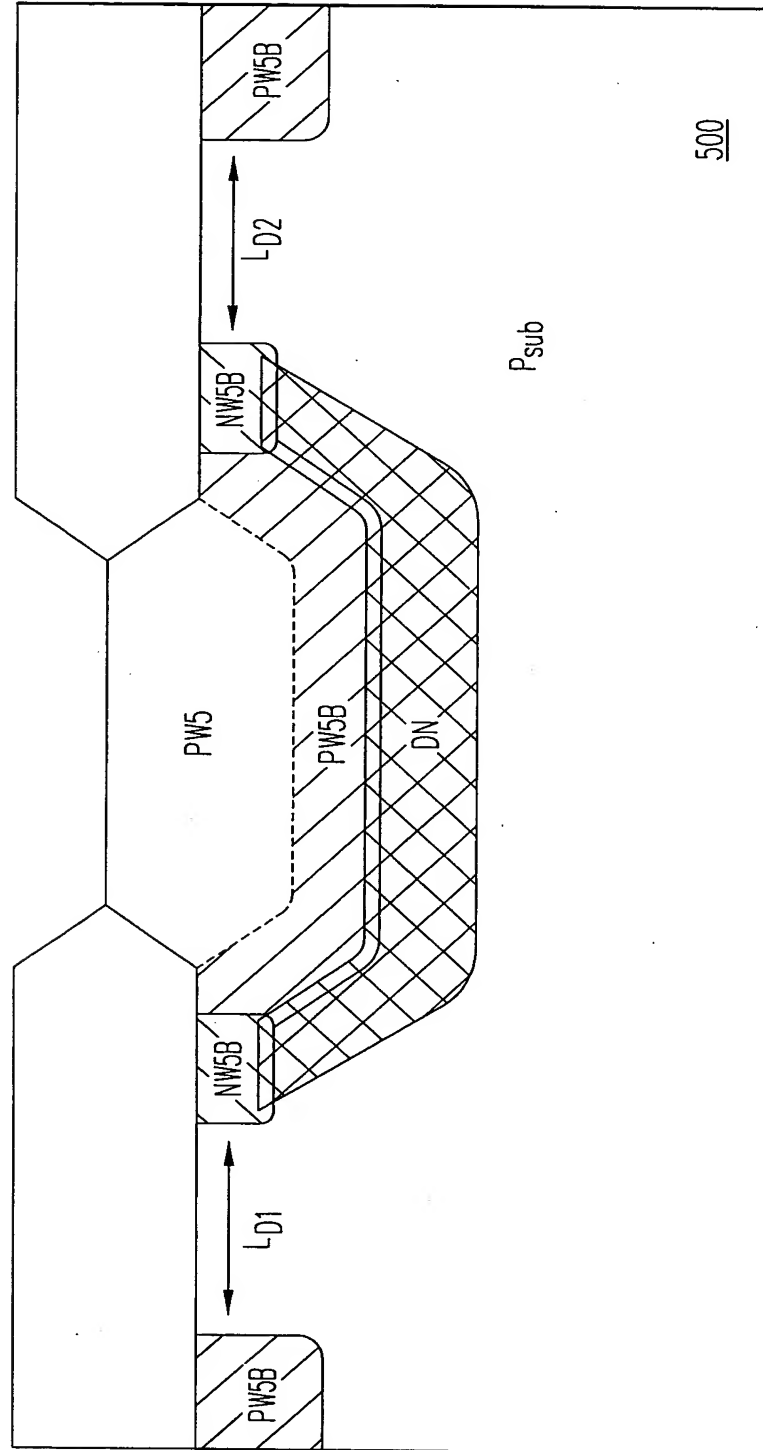


FIG. 14M

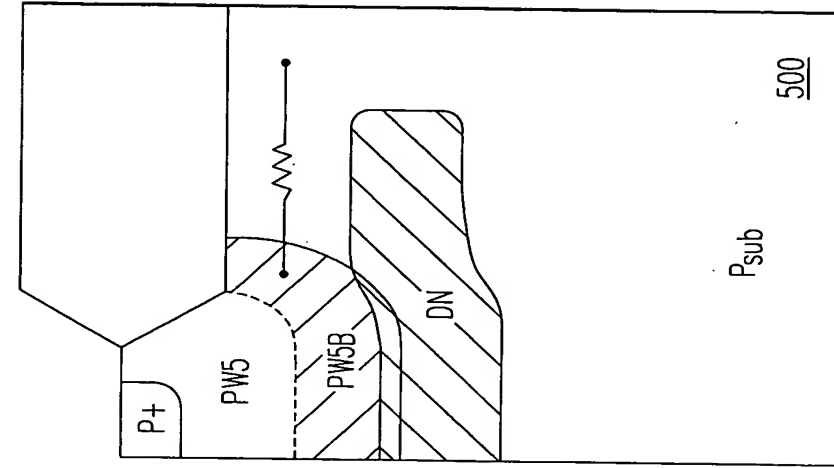


FIG. 14P

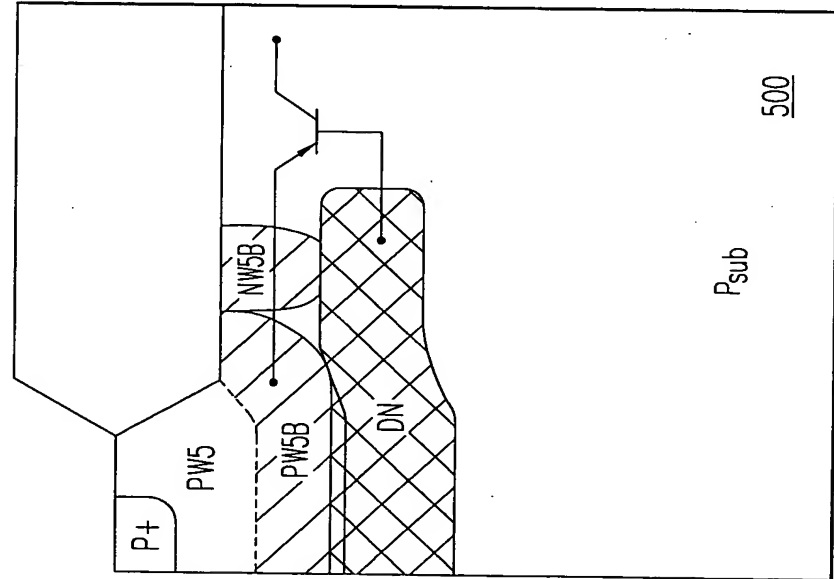


FIG. 14N

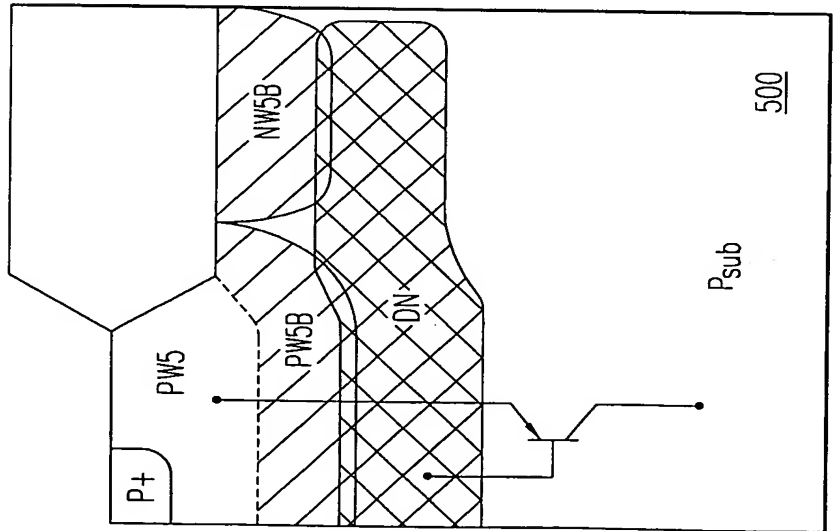


FIG. 14M

FIG. 15A

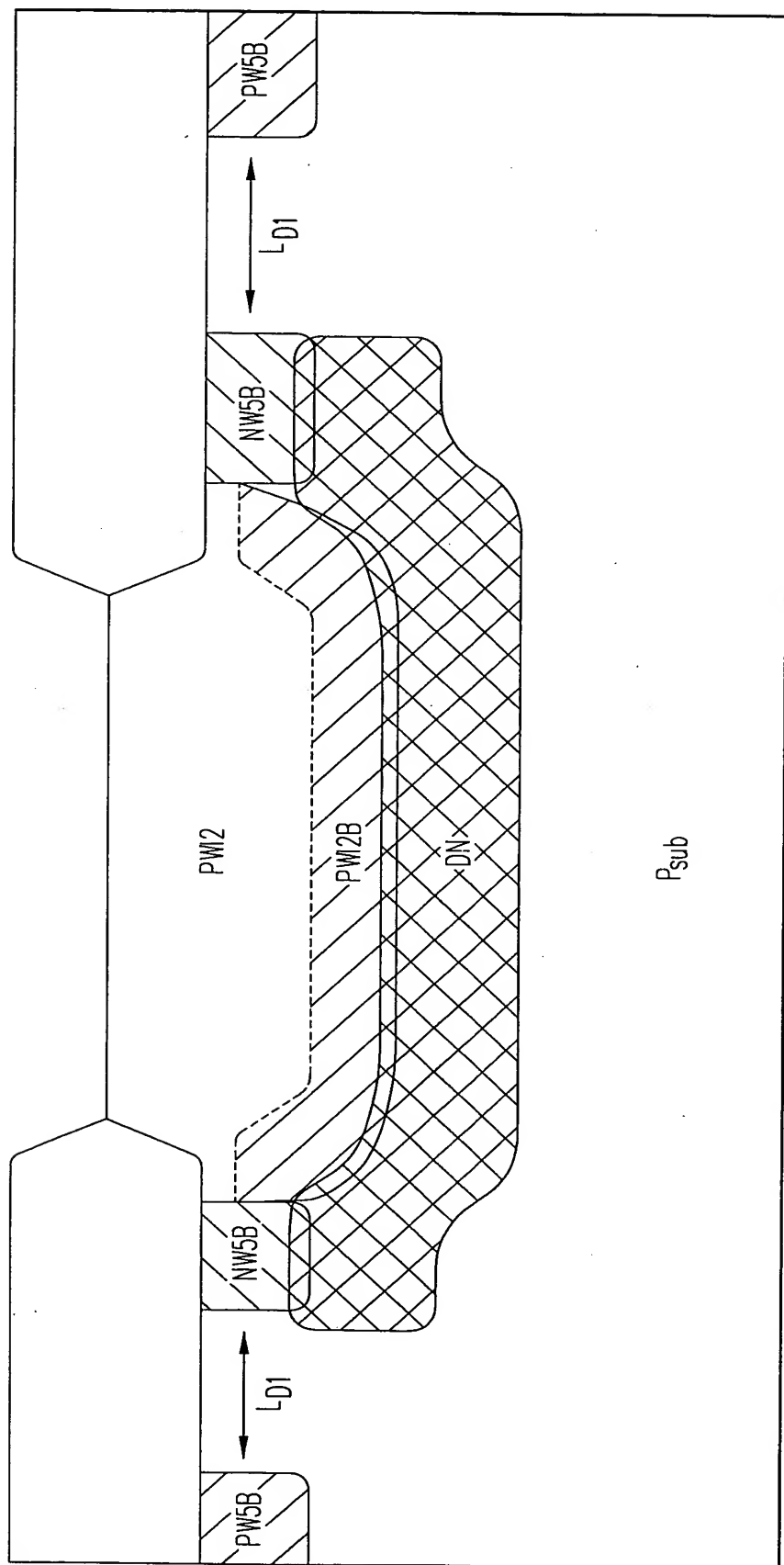


FIG. 15B

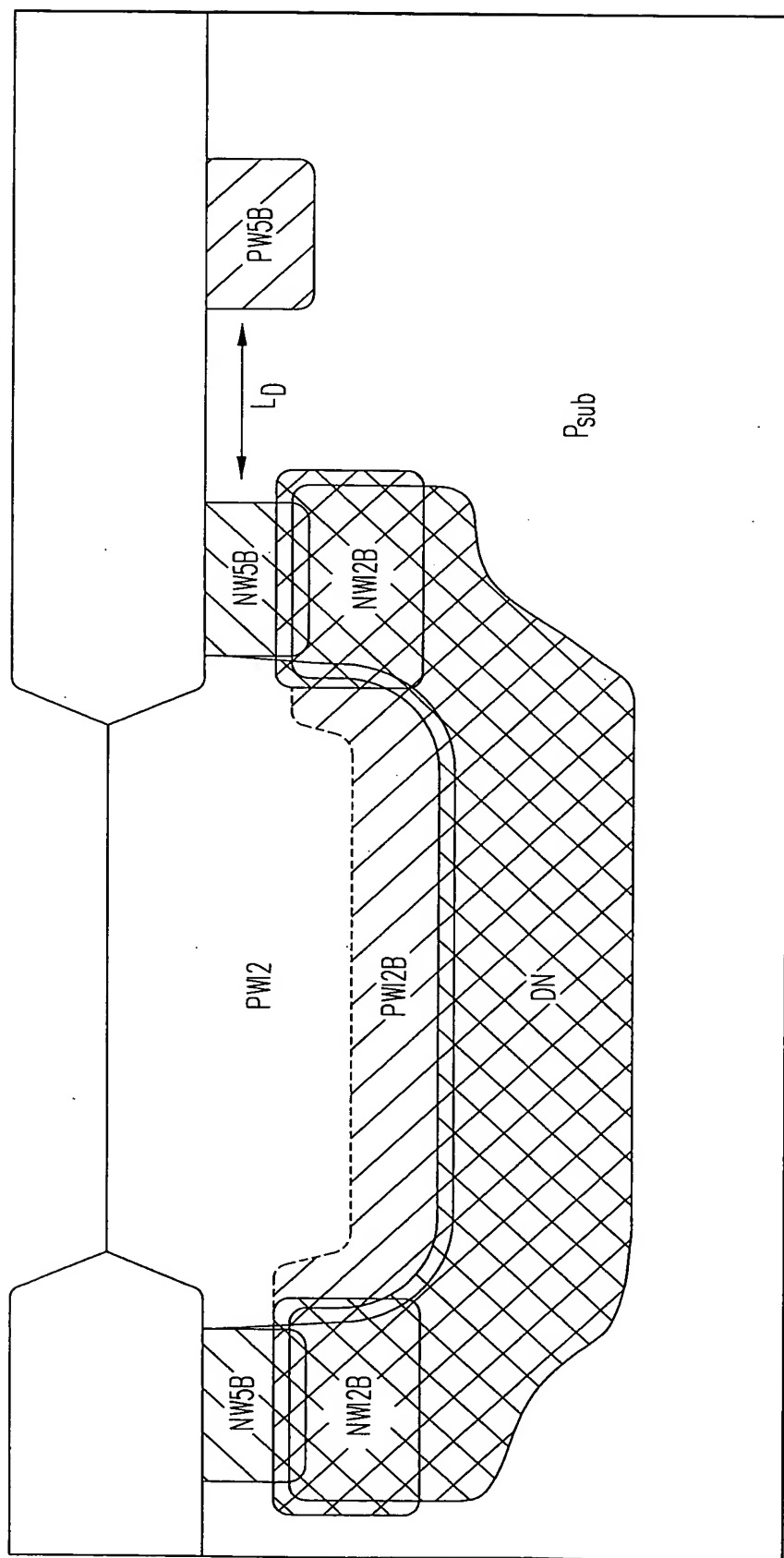


FIG. 15C

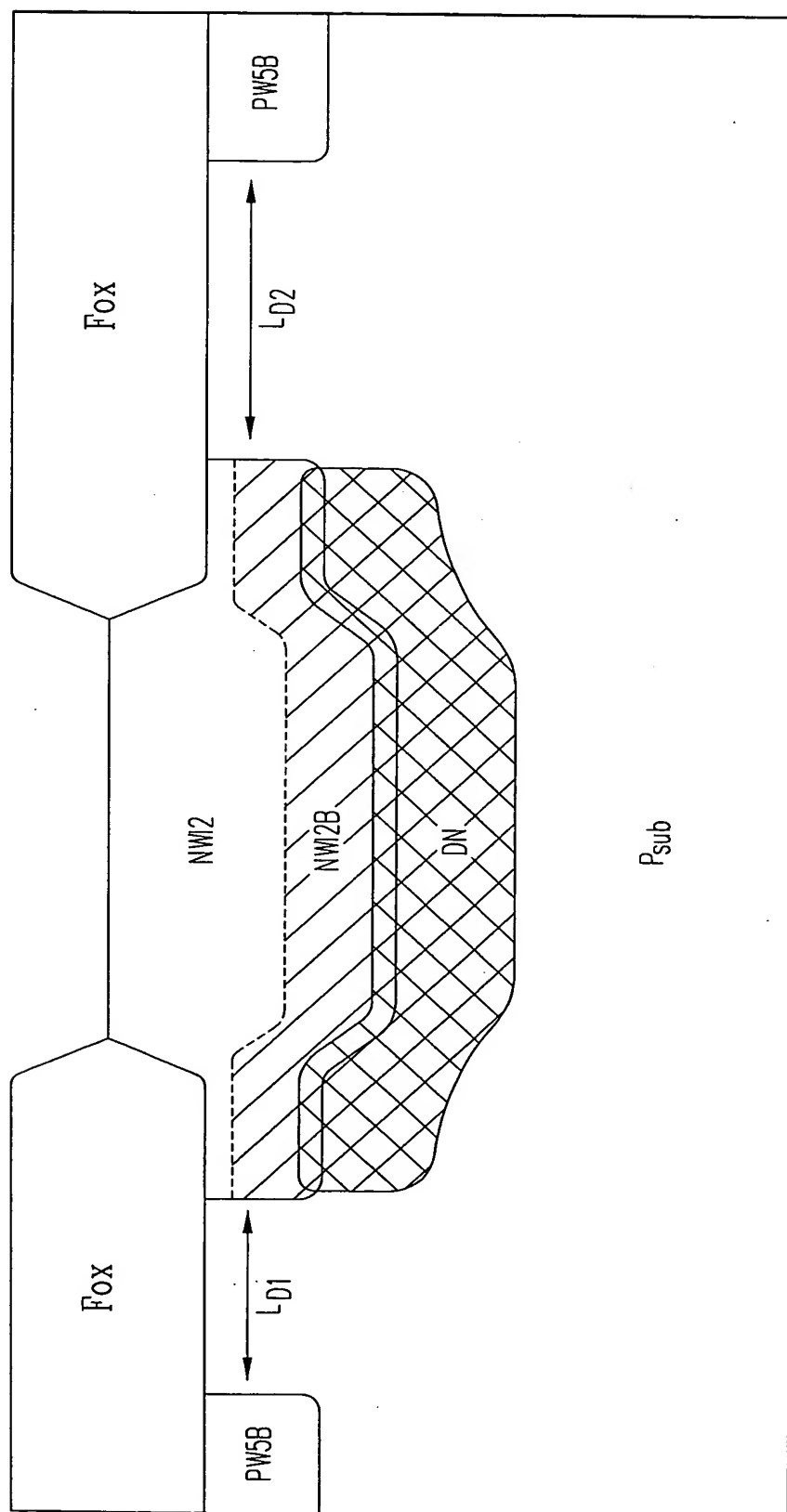


FIG. 15D

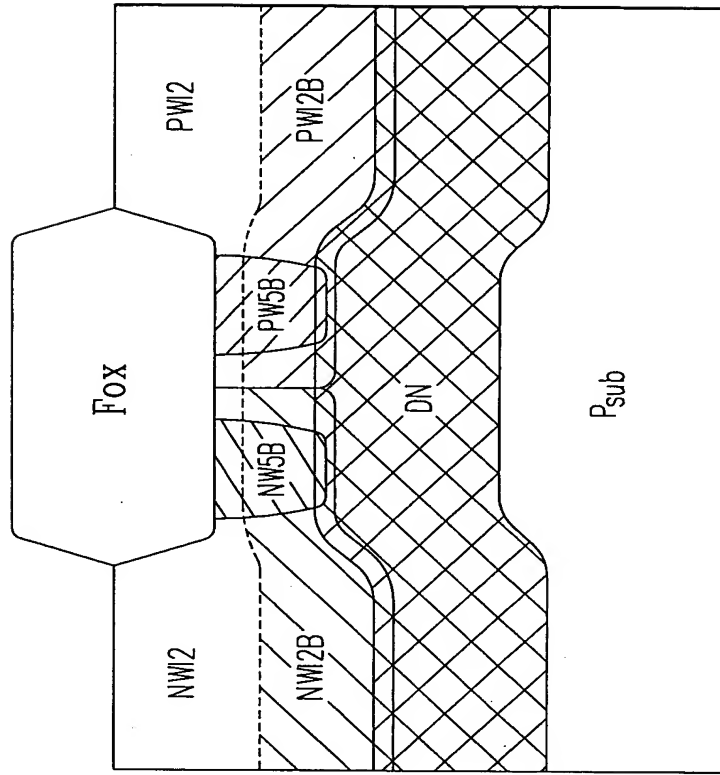


FIG. 15F

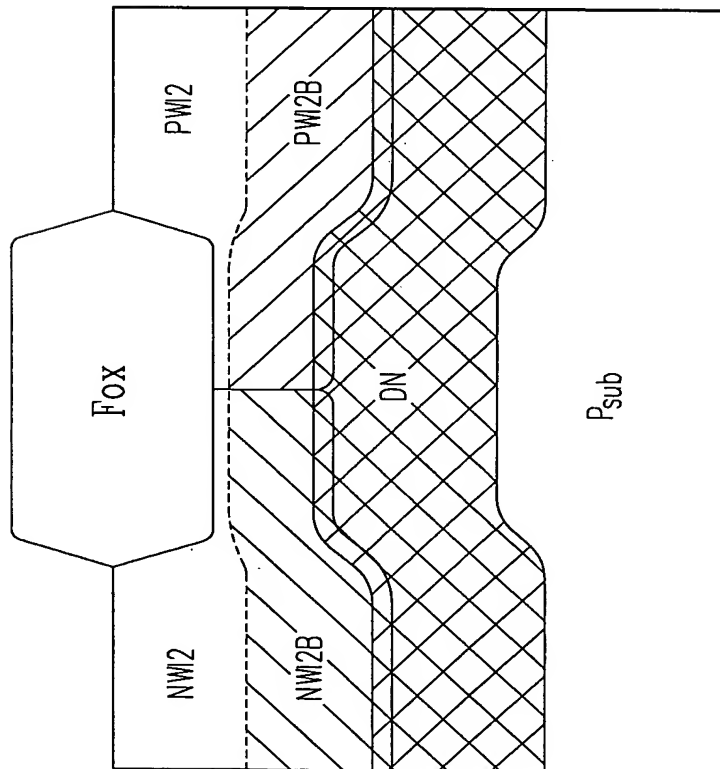


FIG. 15E

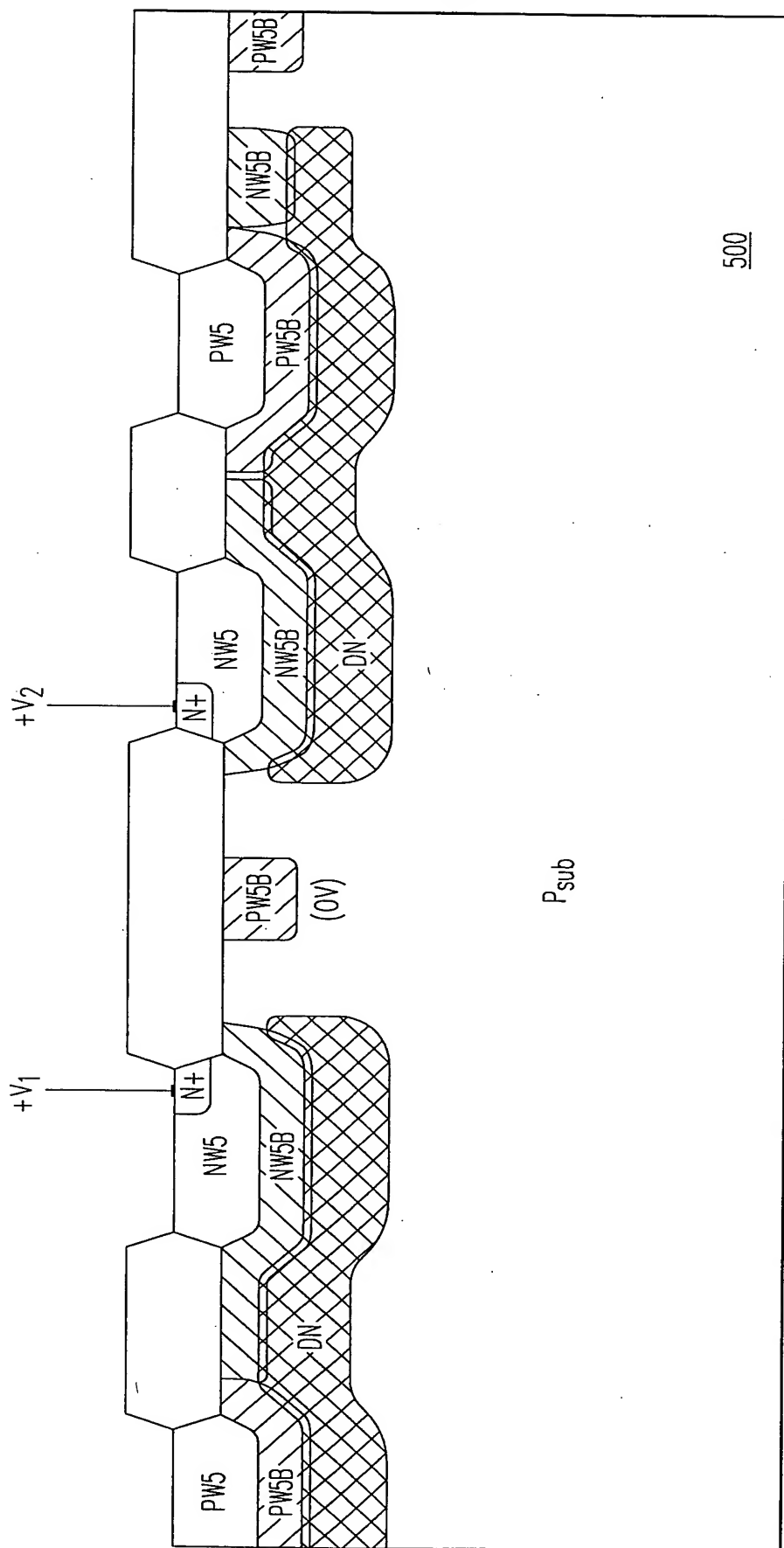


FIG. 16A



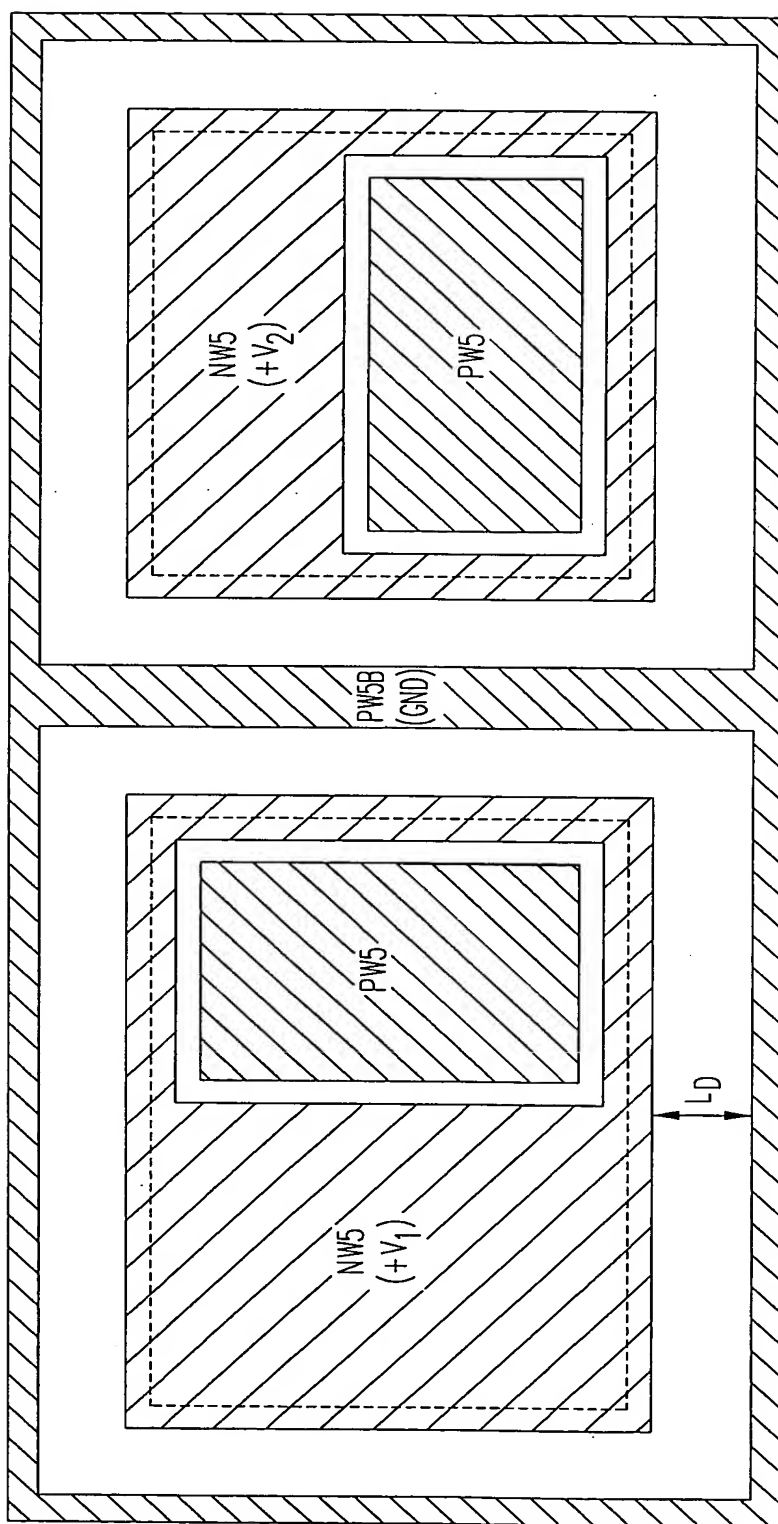
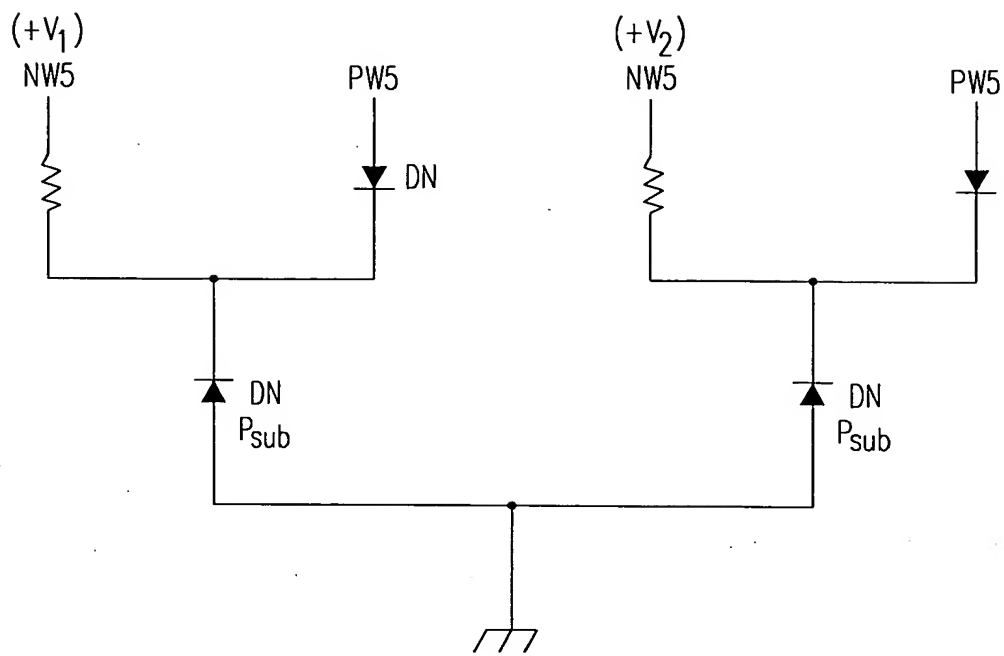
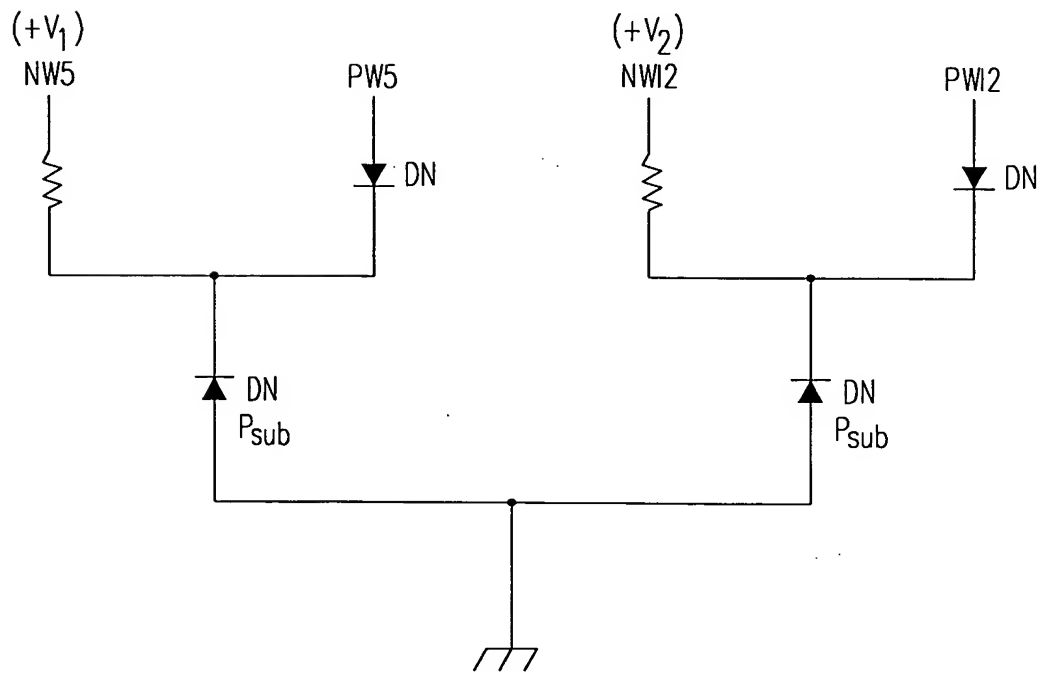


FIG. 16B

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*FIG. 16C*



*FIG. 16E*

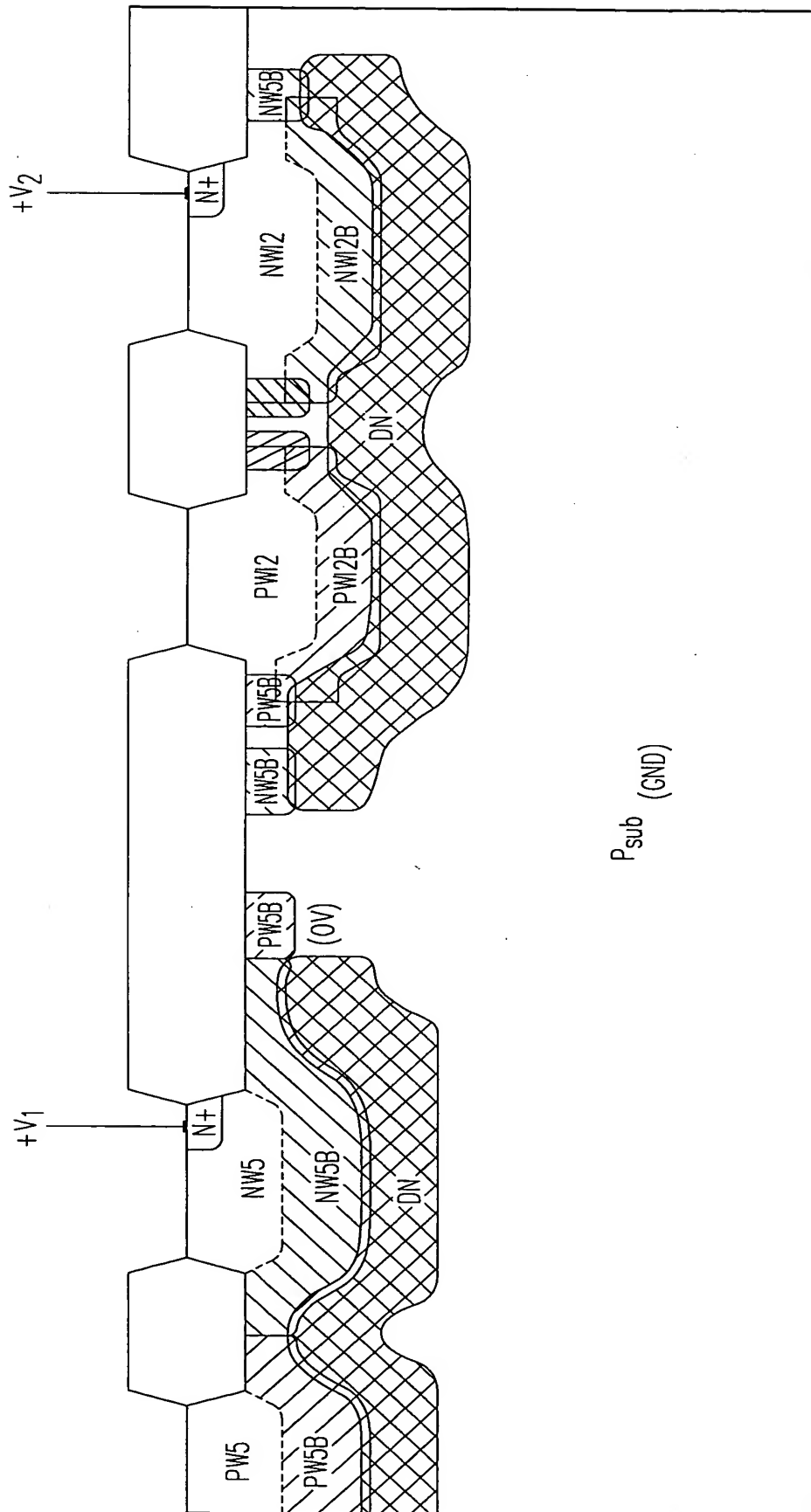


FIG. 16D

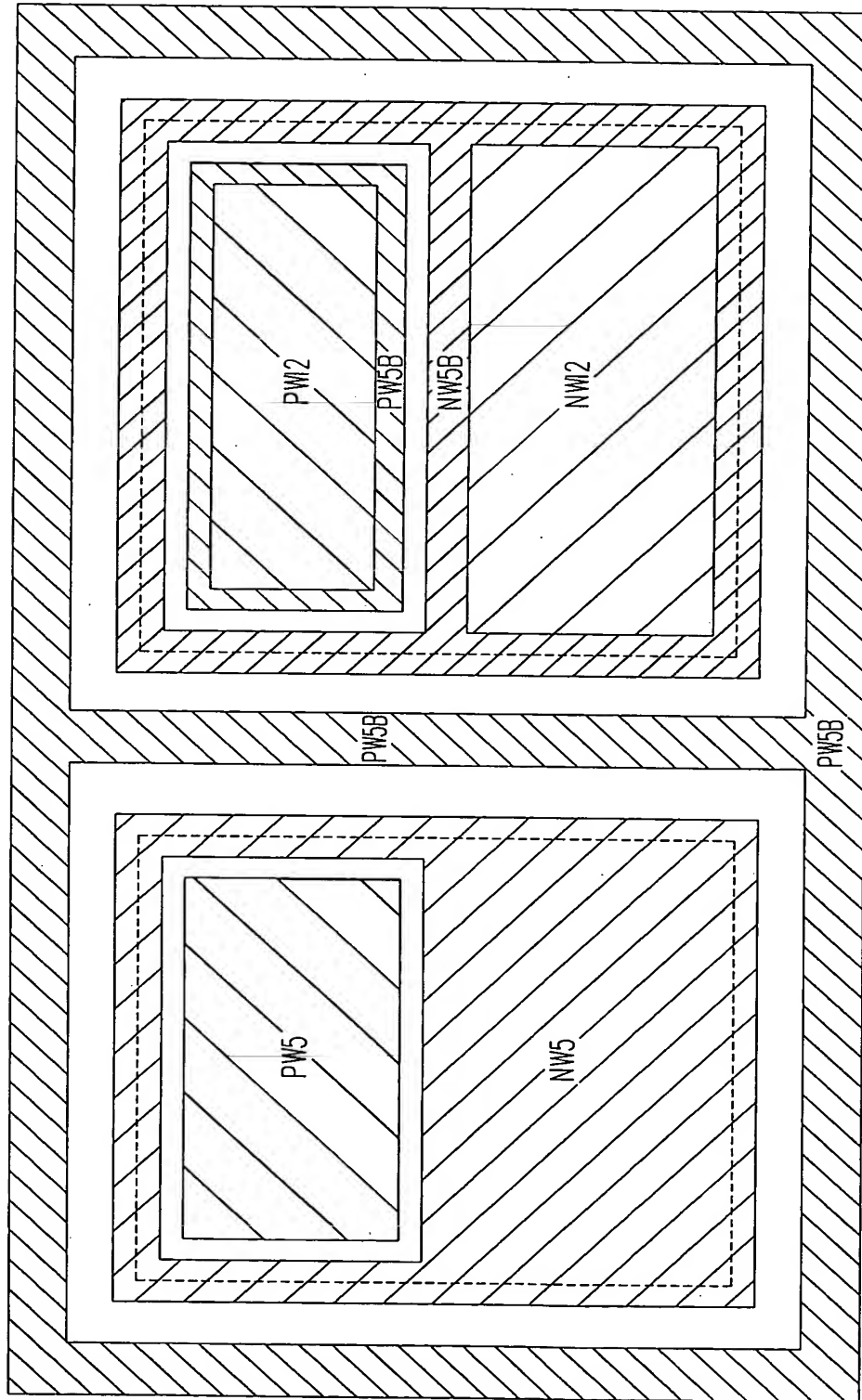
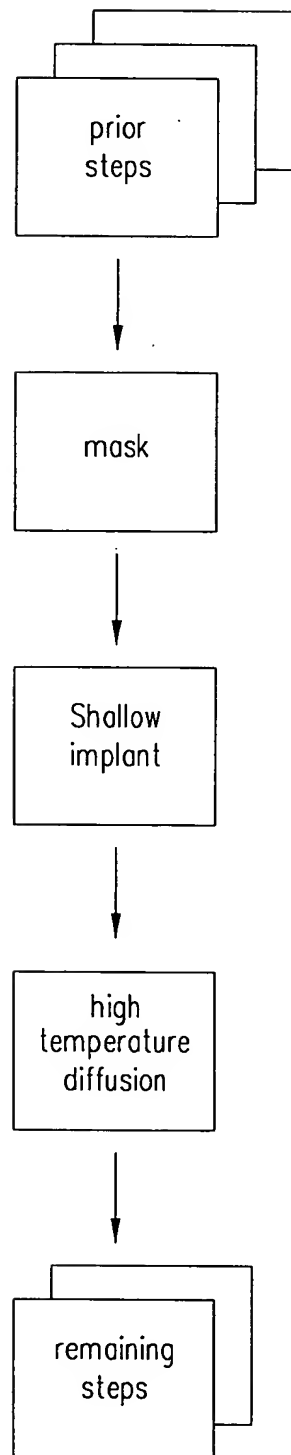
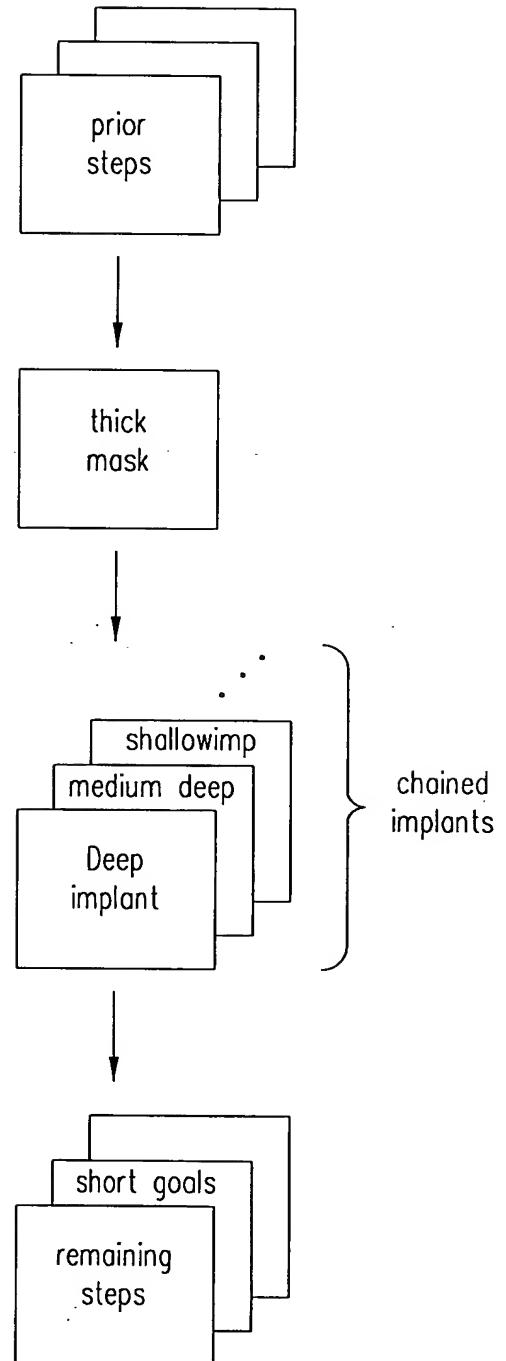


FIG. 16F



**FIG. 17A**  
(Prior Art)



**FIG. 17B**

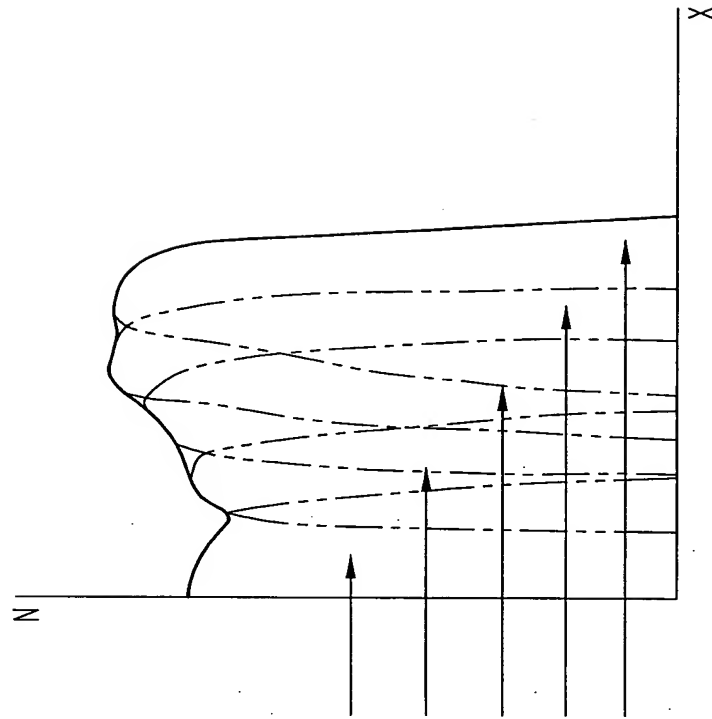


FIG. 17D

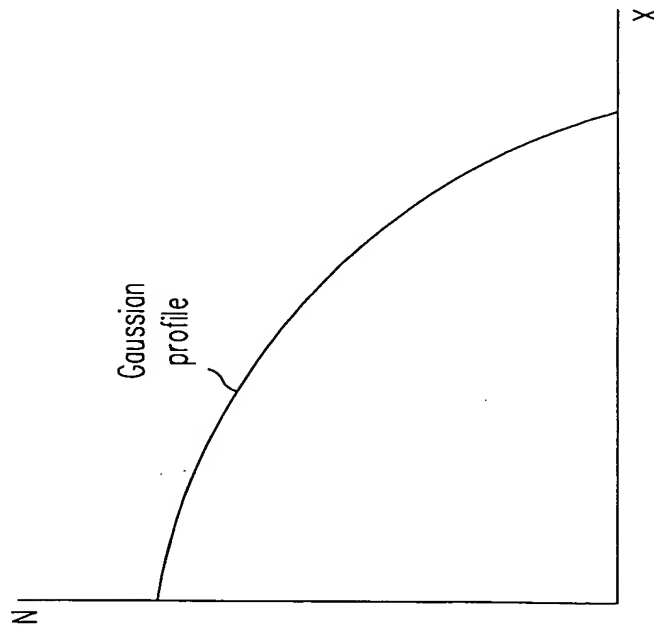


FIG. 17C

(Prior Art)

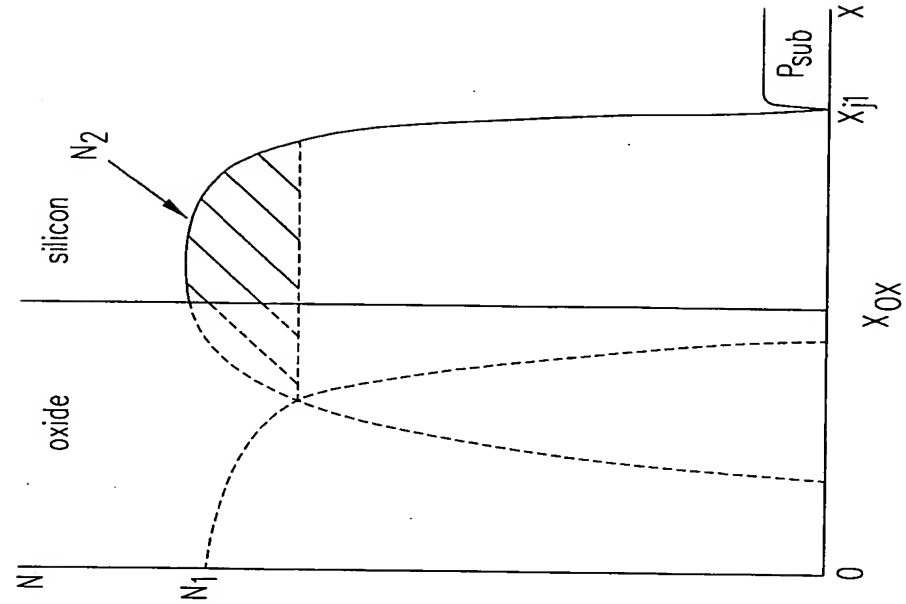


FIG. 17E

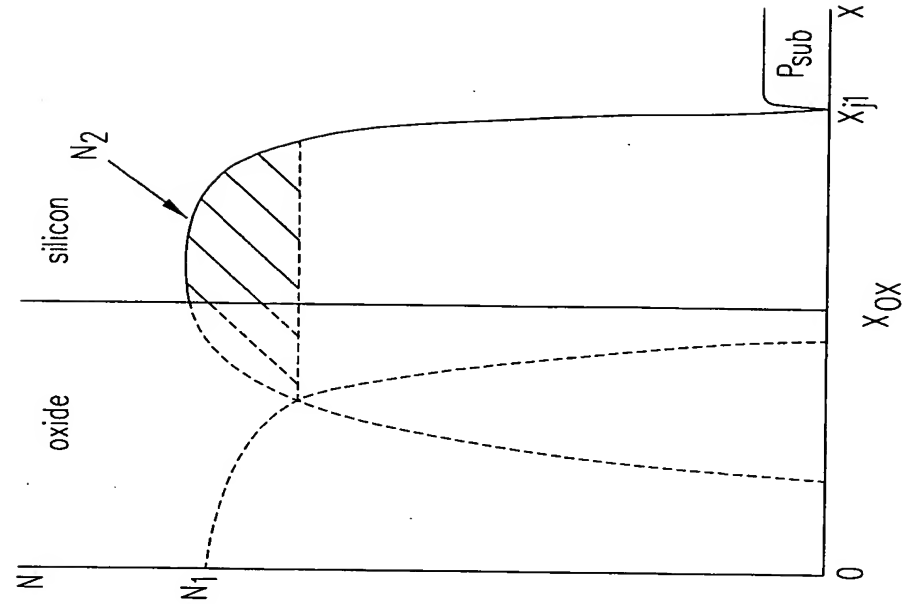


FIG. 17F

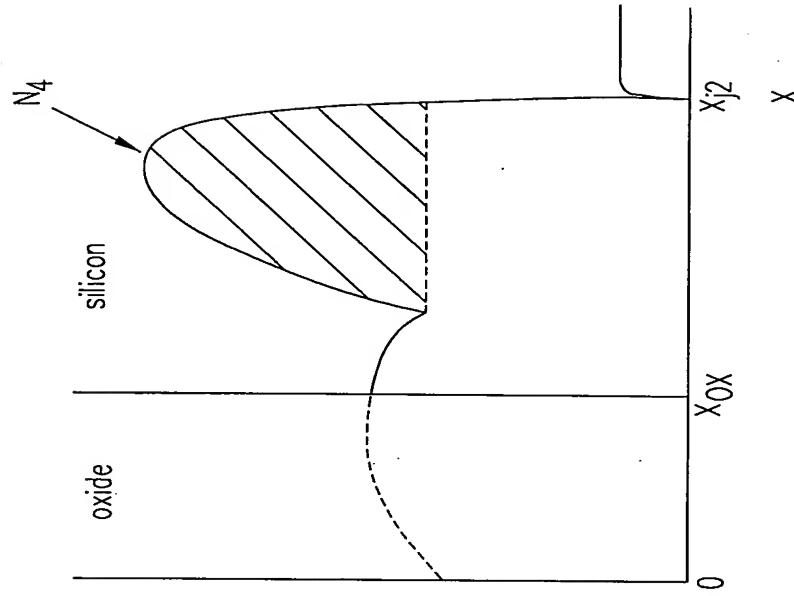


FIG. 17H

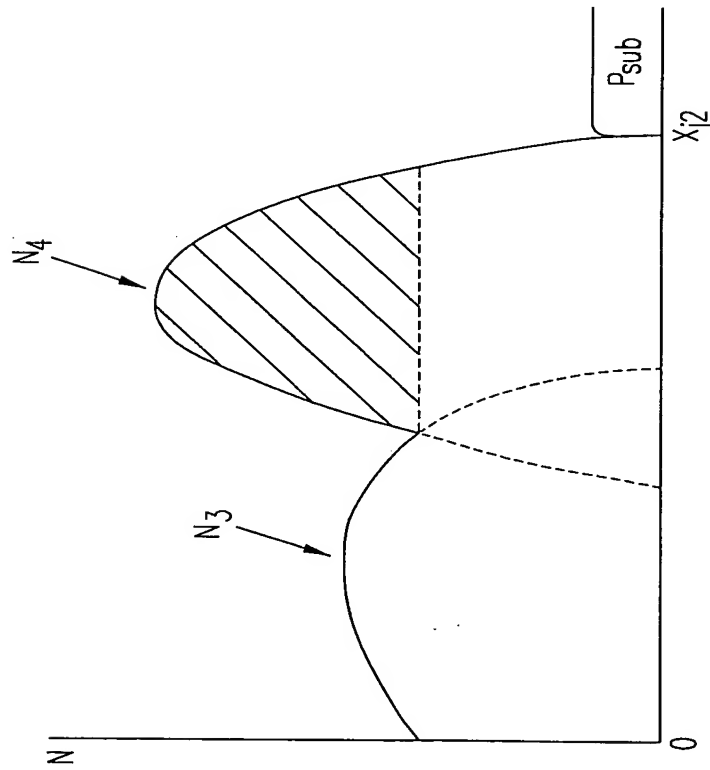


FIG. 17G



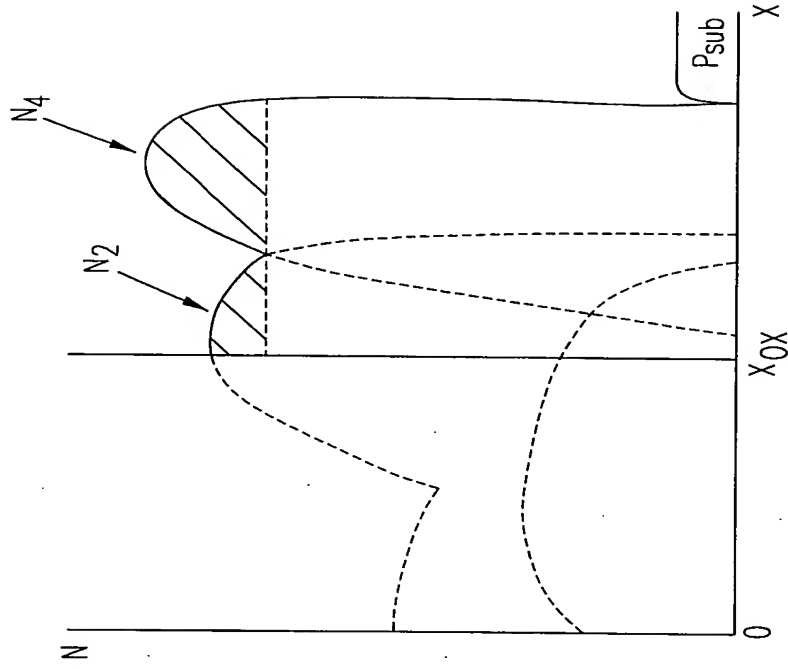


FIG. 17J

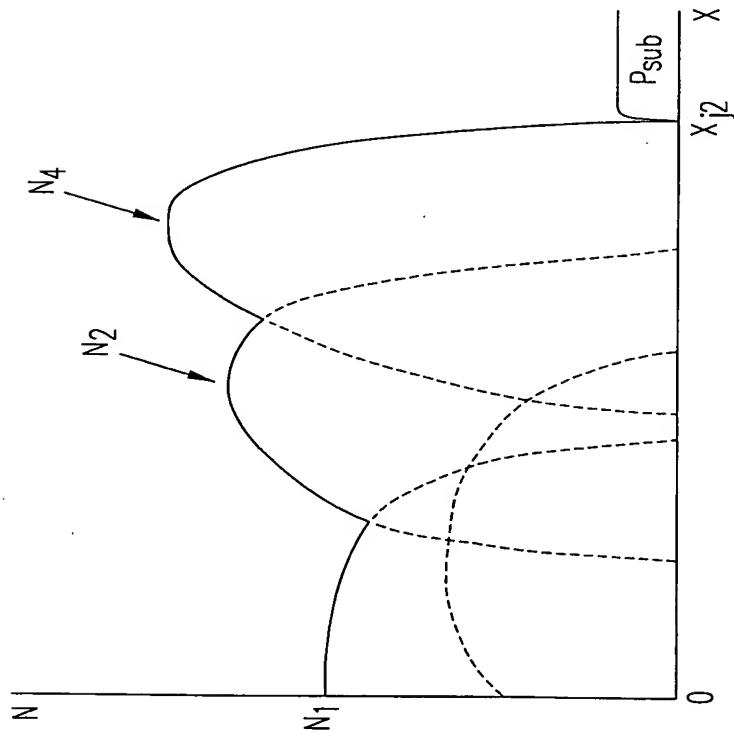


FIG. 17I

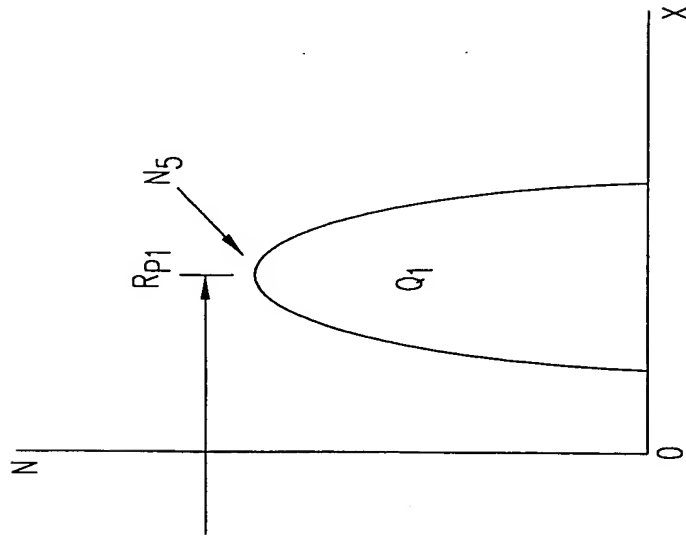


FIG. 17K  
(Prior Art)

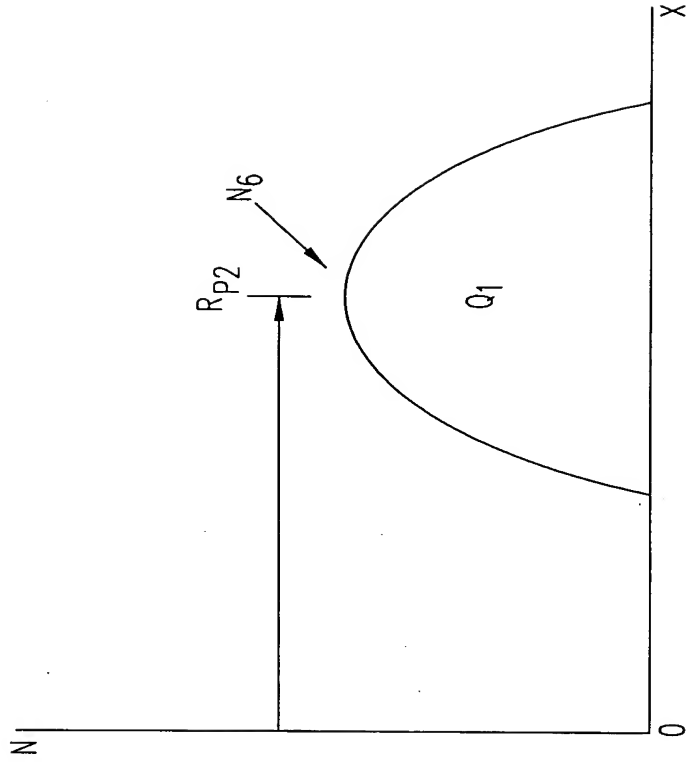


FIG. 17L  
(Prior Art)

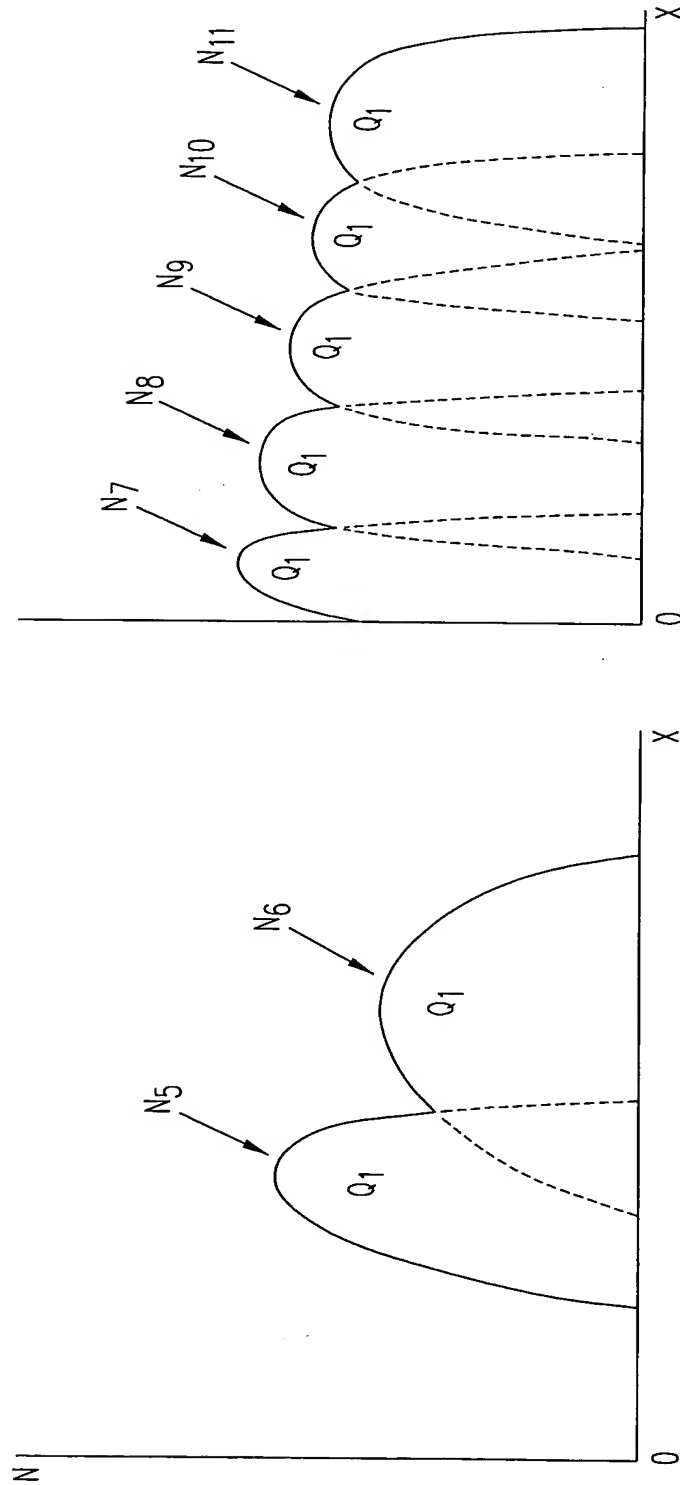


FIG. 17N

FIG. 17M

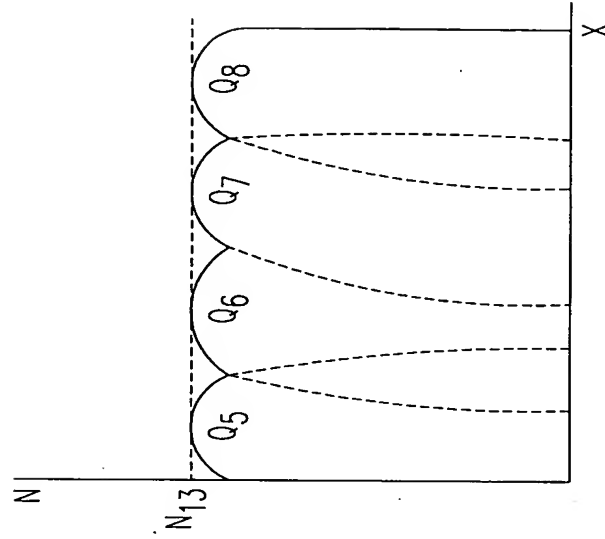


FIG. 170

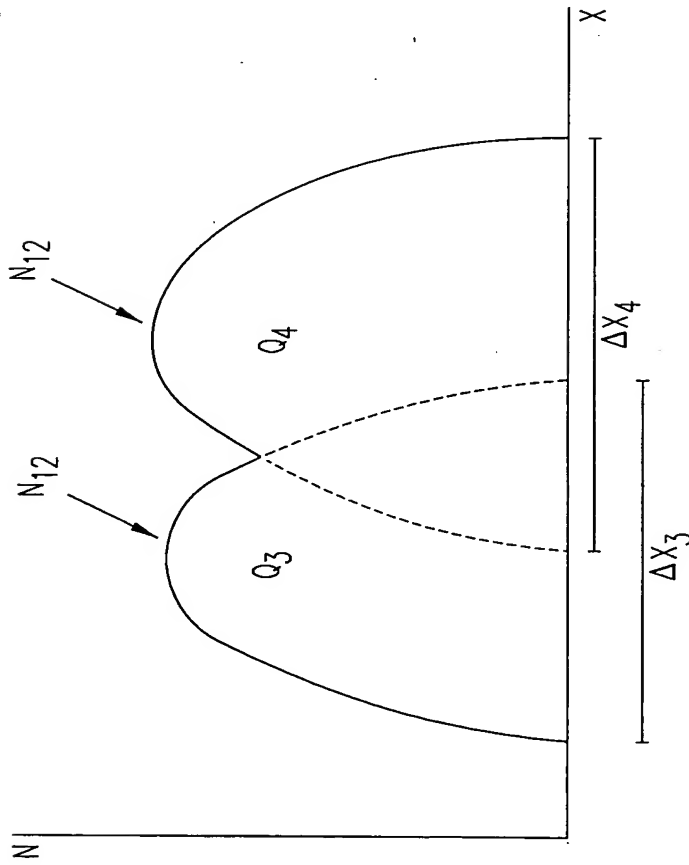


FIG. 17P

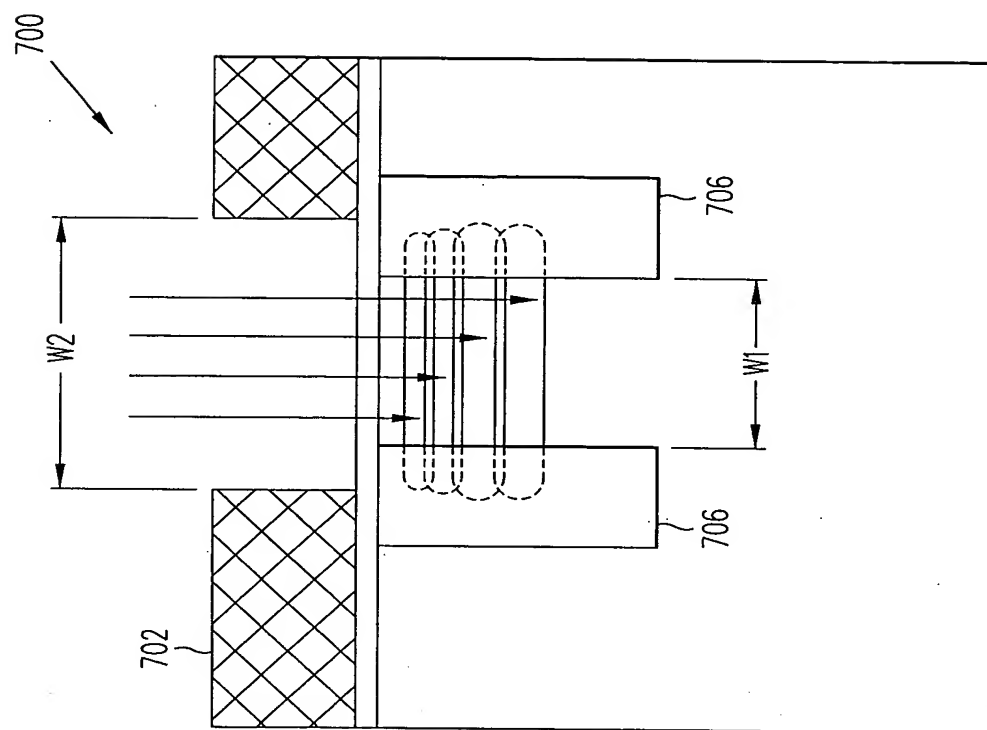


FIG. 17R

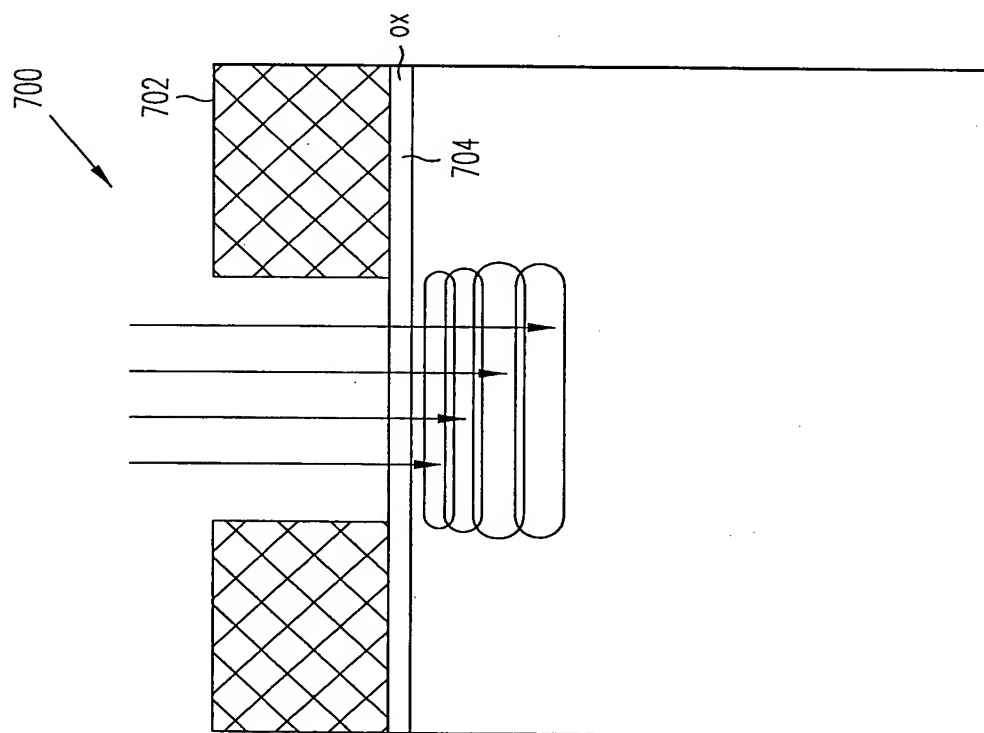


FIG. 17Q

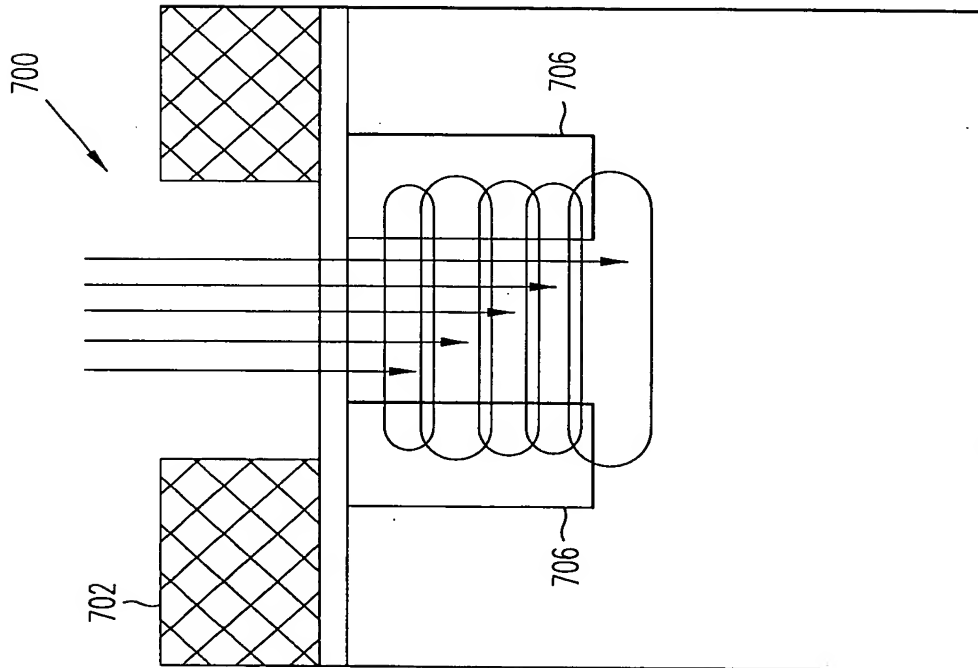


FIG. 17S

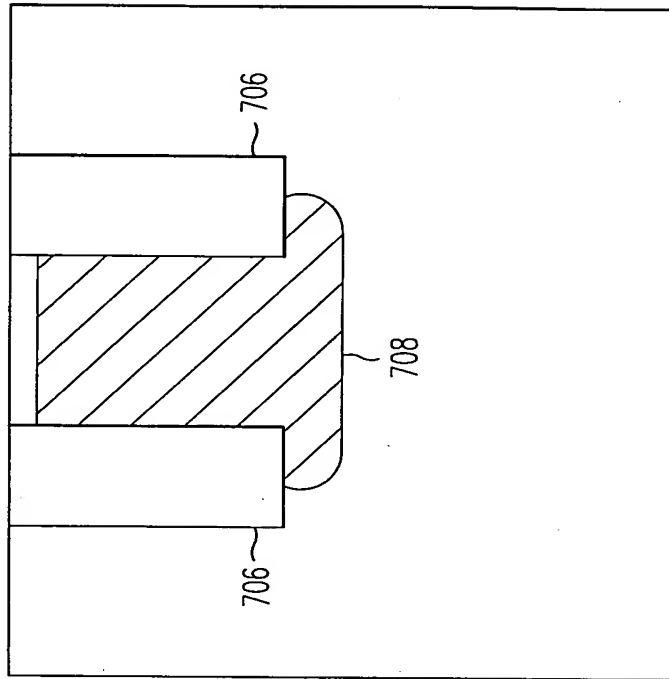


FIG. 17T

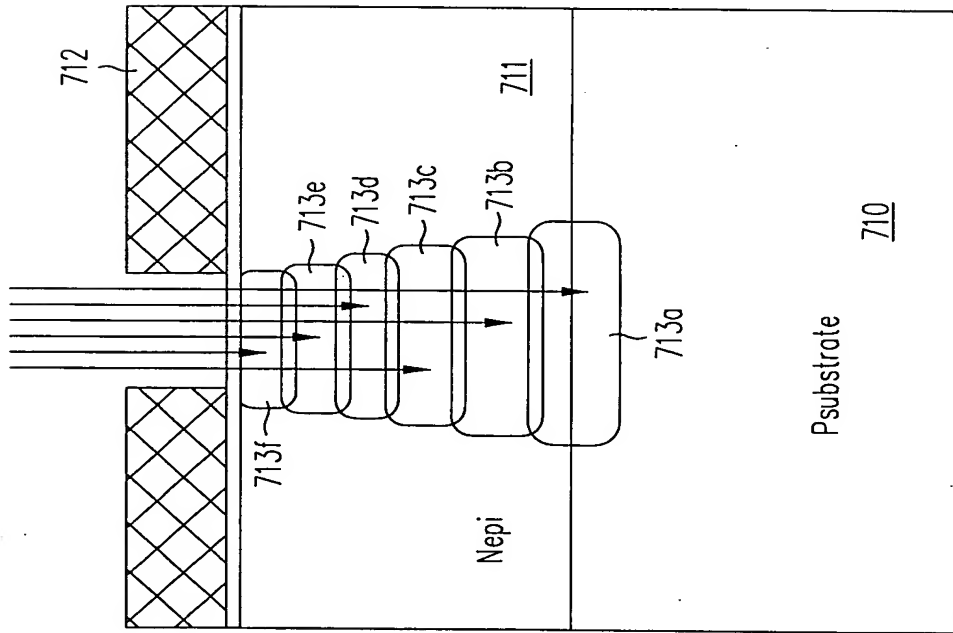


FIG. 17U

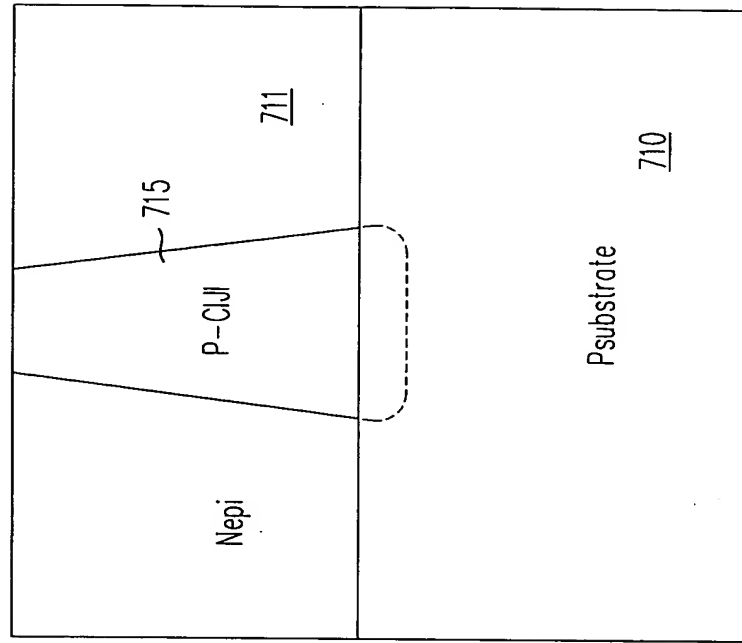


FIG. 17V

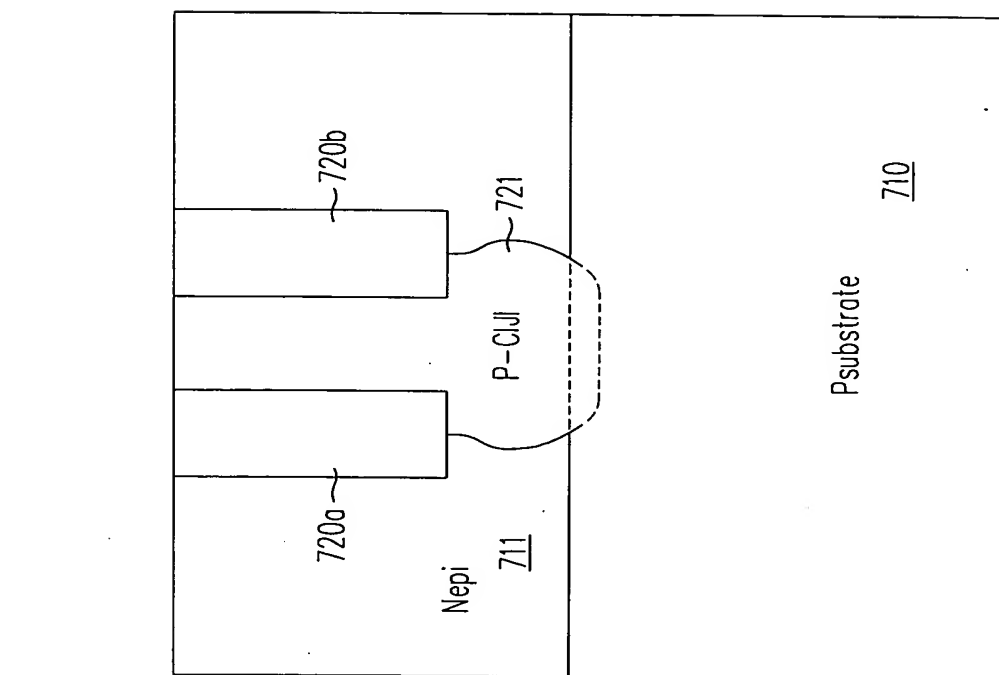


FIG. 17X

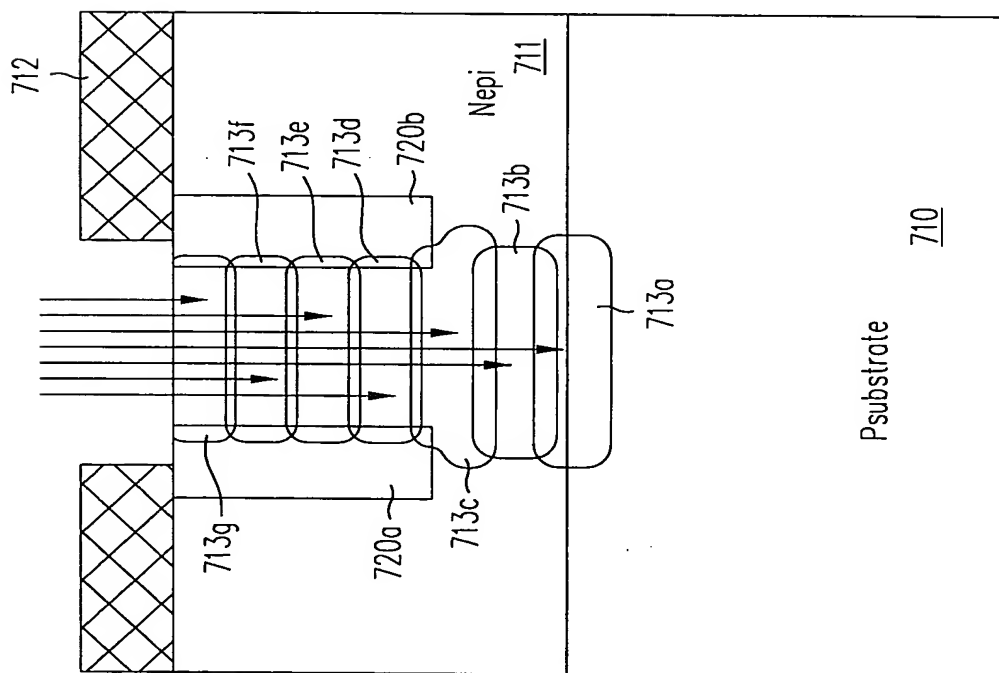


FIG. 17W



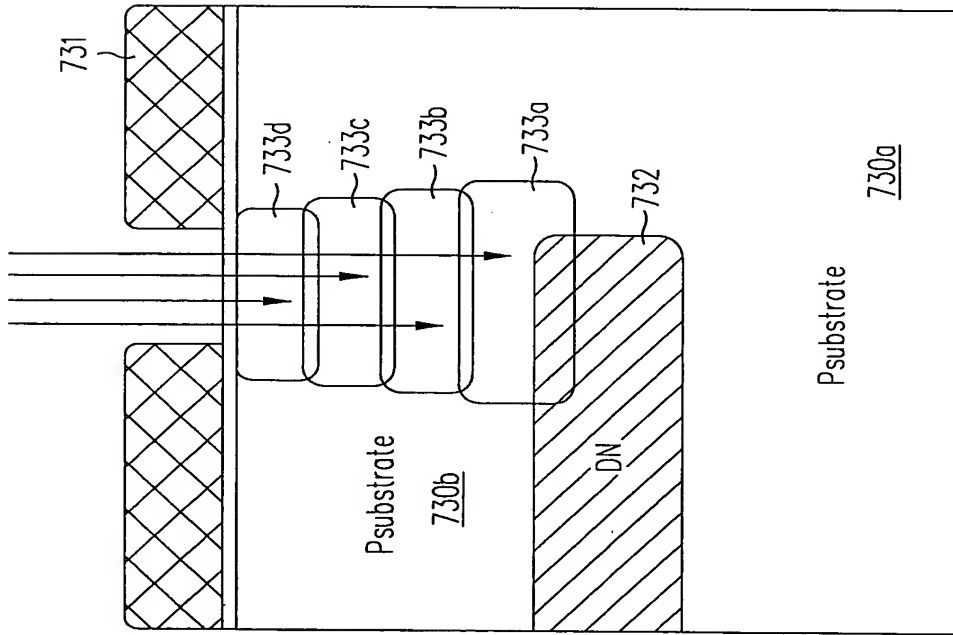


FIG. 17Y

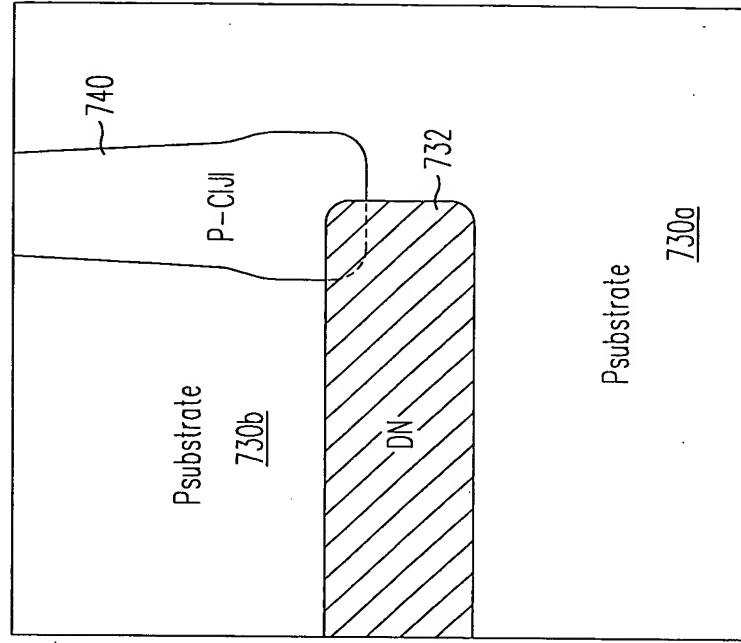


FIG. 17Z

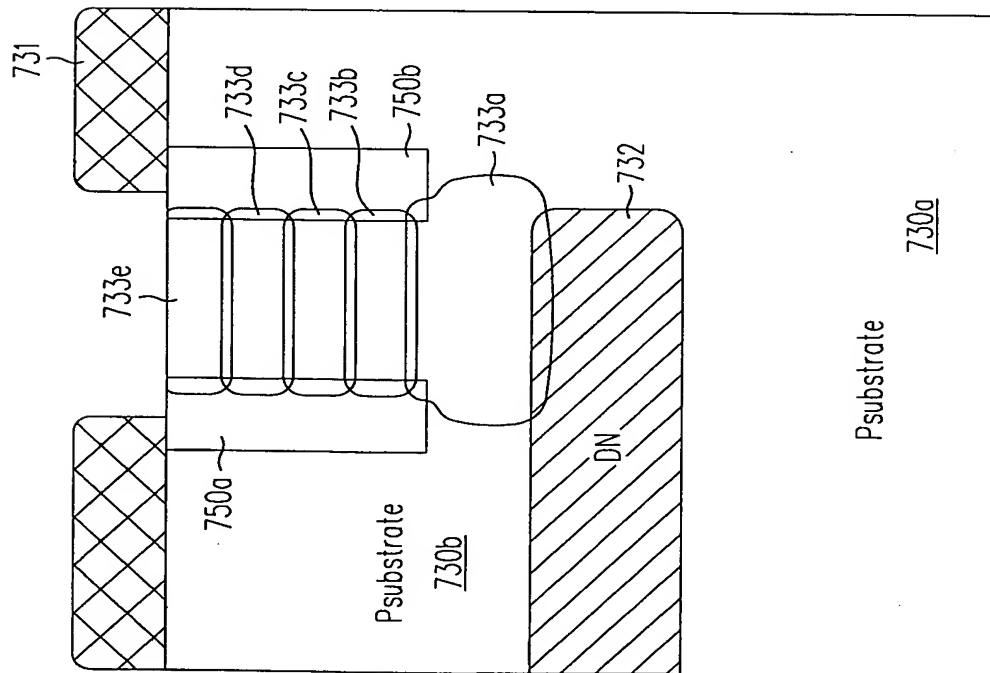


FIG. 17AA

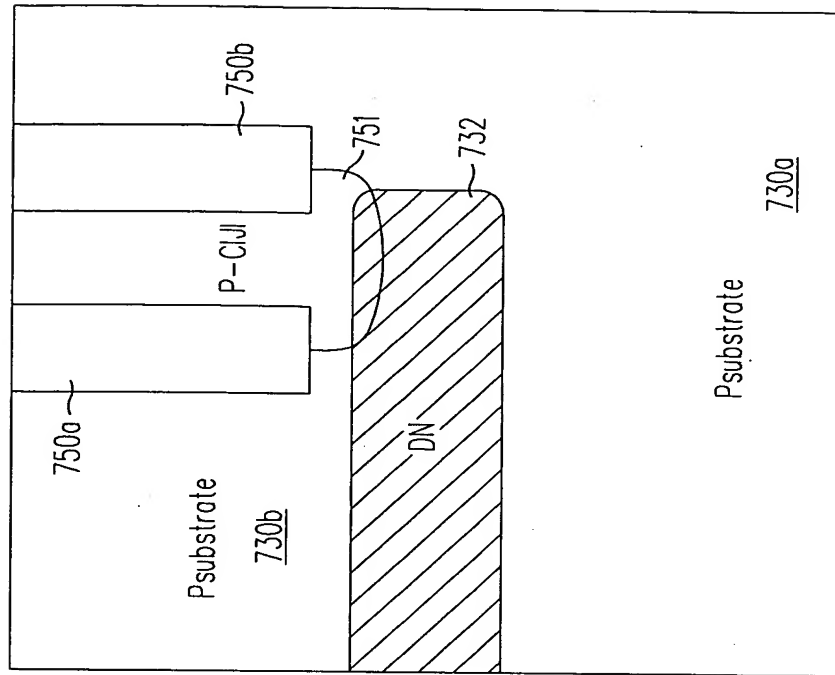


FIG. 17BB

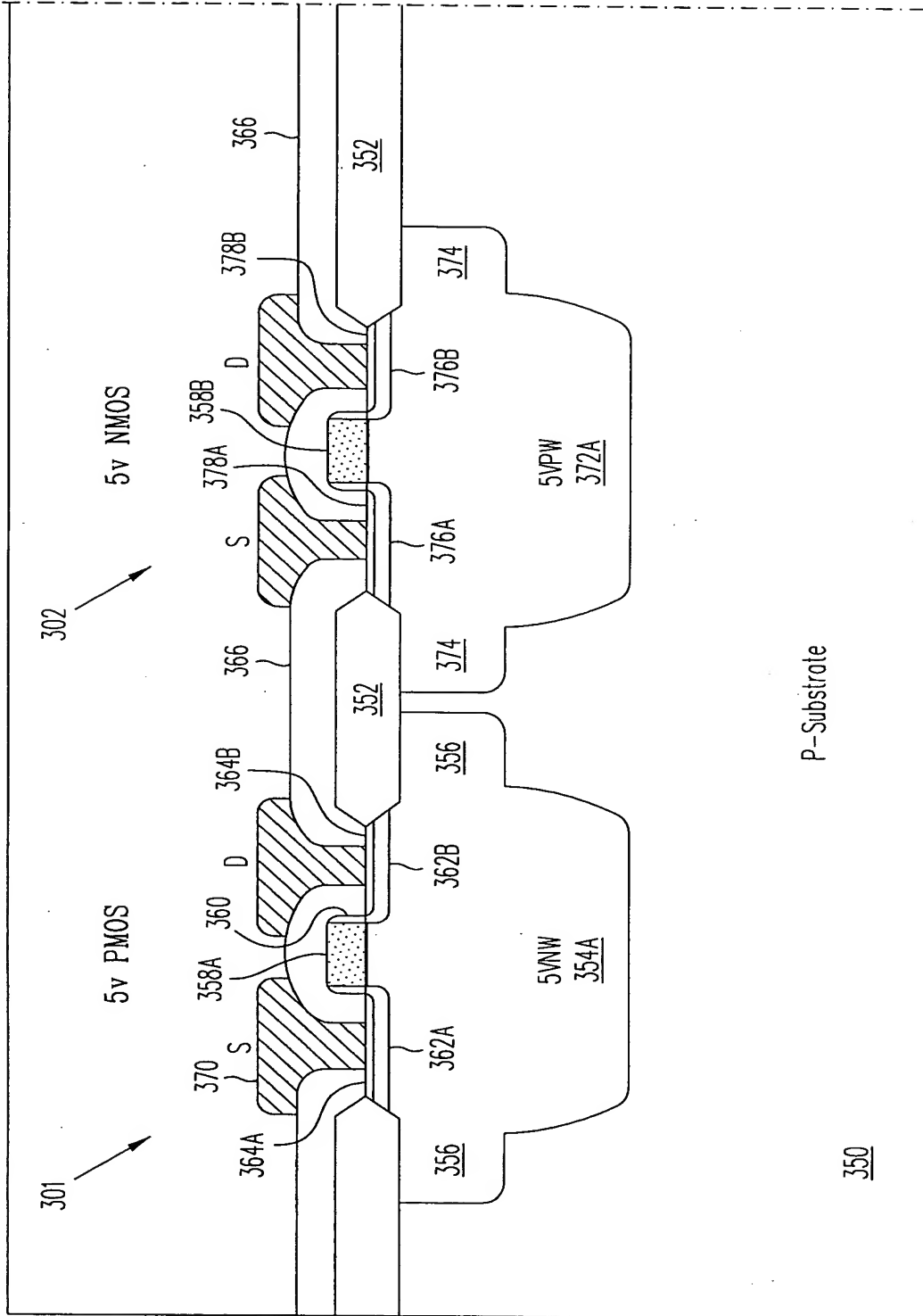


FIG. 18A-1	FIG. 18A-2
FIG. 18A-3	FIG. 18A-4

Key To  
**FIG. 18A**

**FIG. 18A-1**

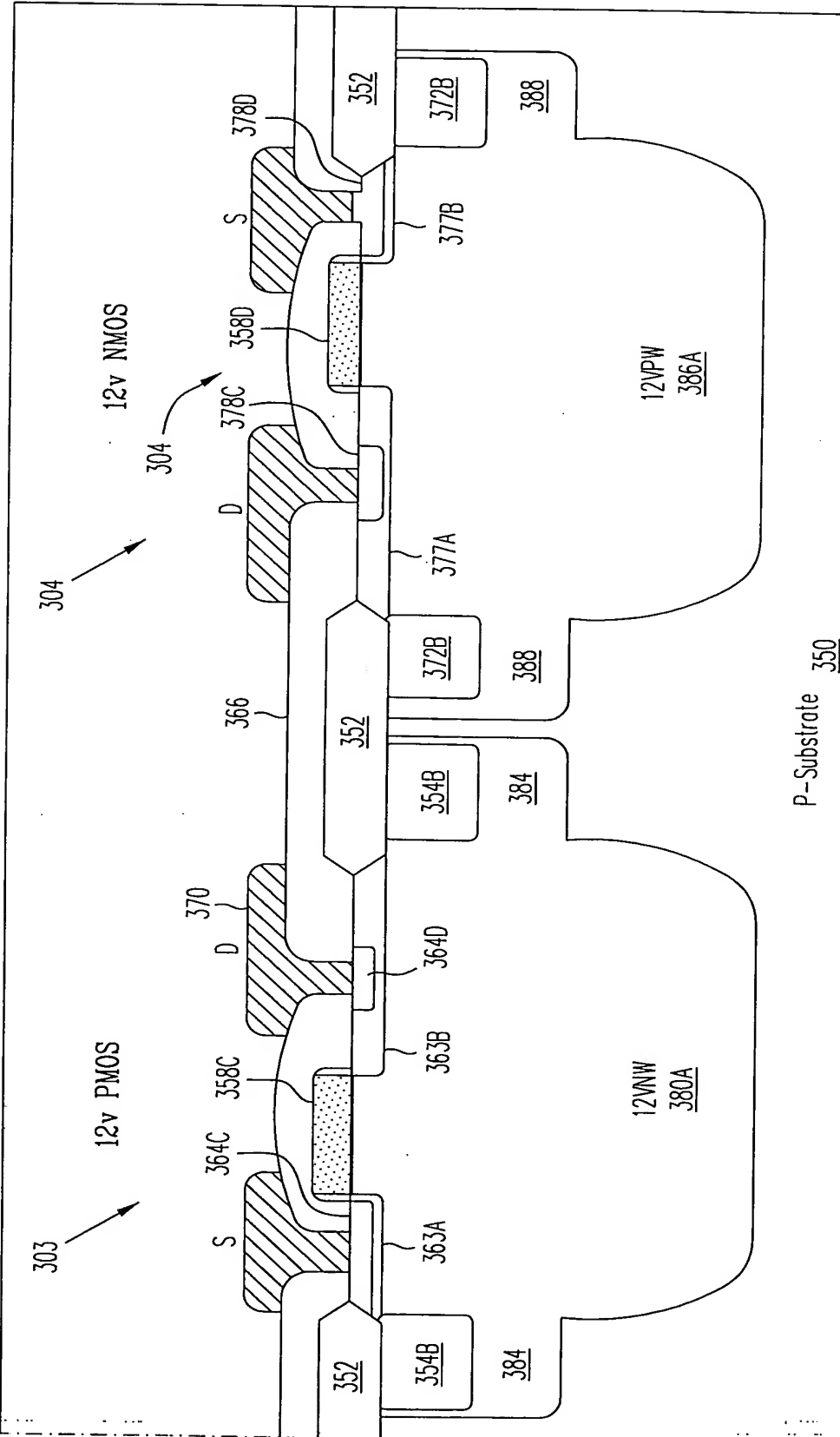


FIG. 18A-2

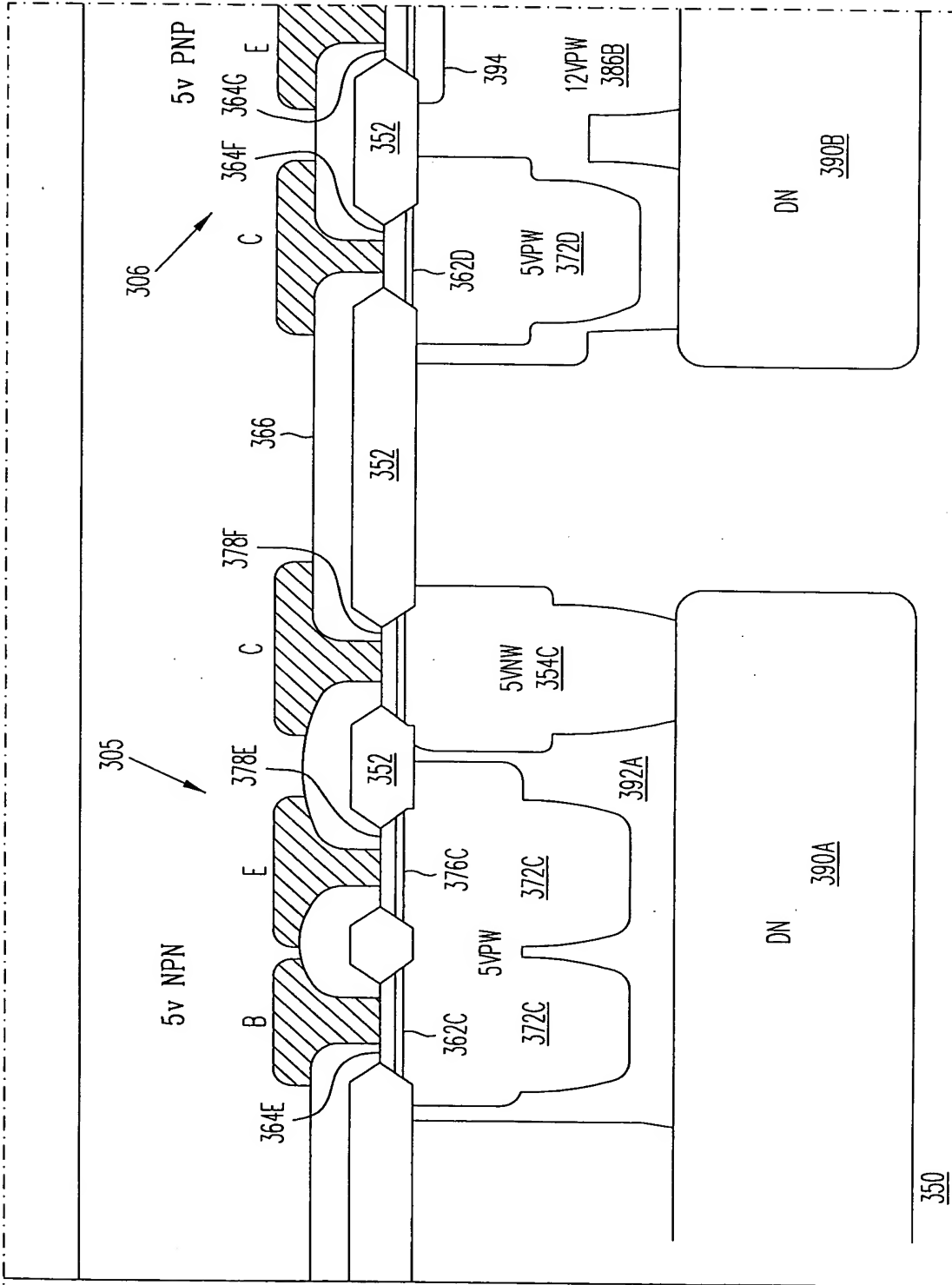


FIG. 18A-3

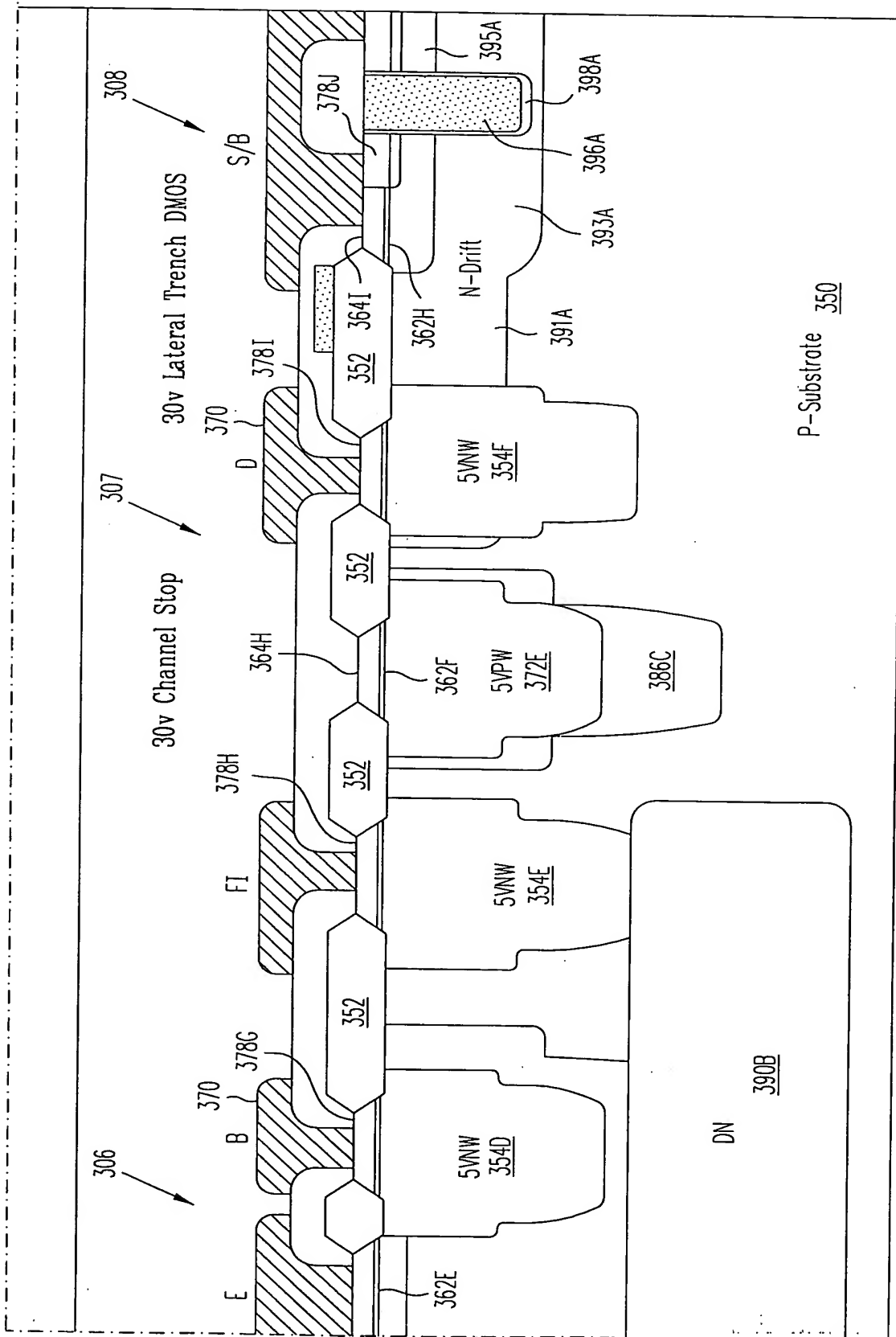
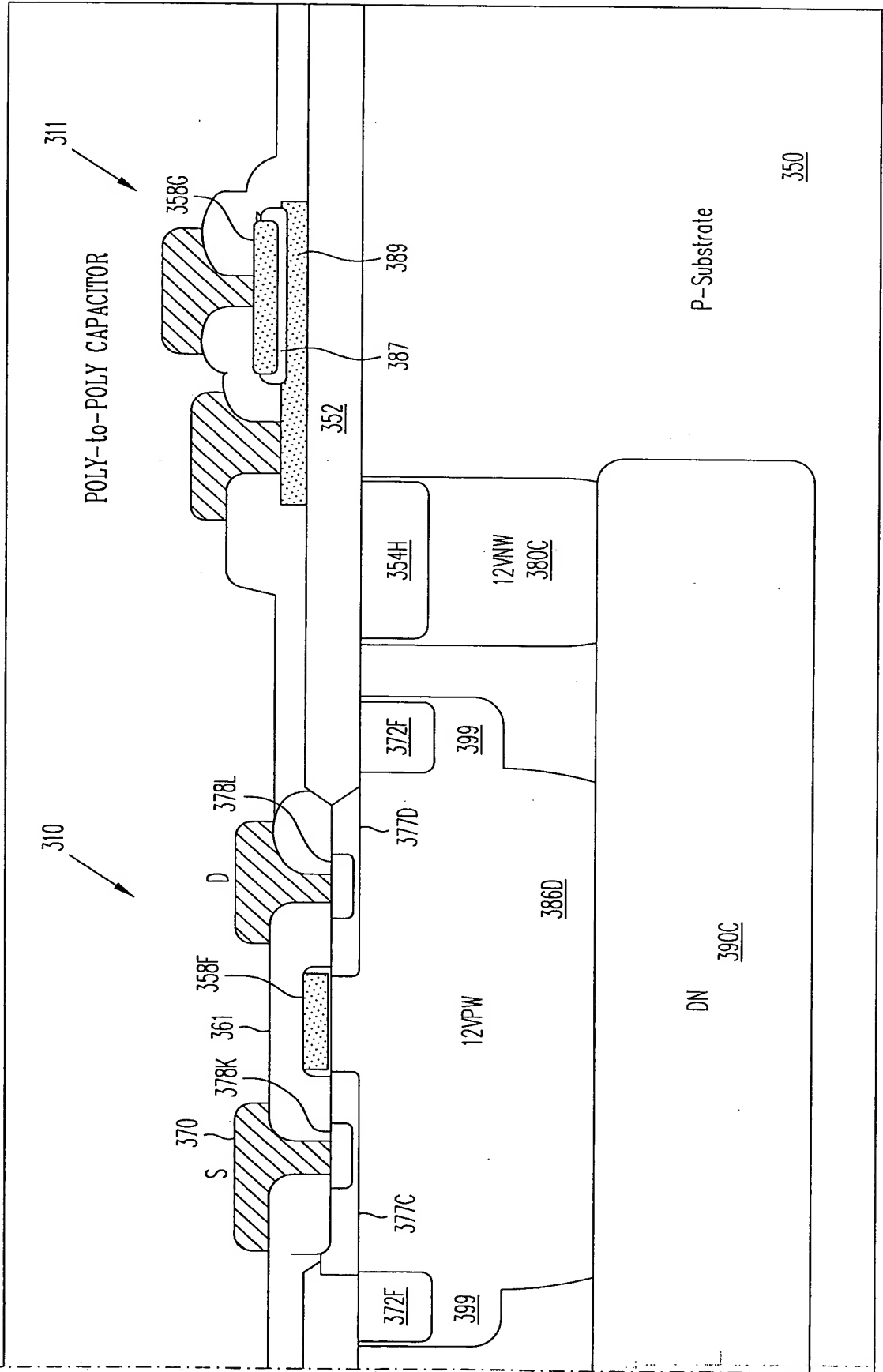




FIG. 18B-2







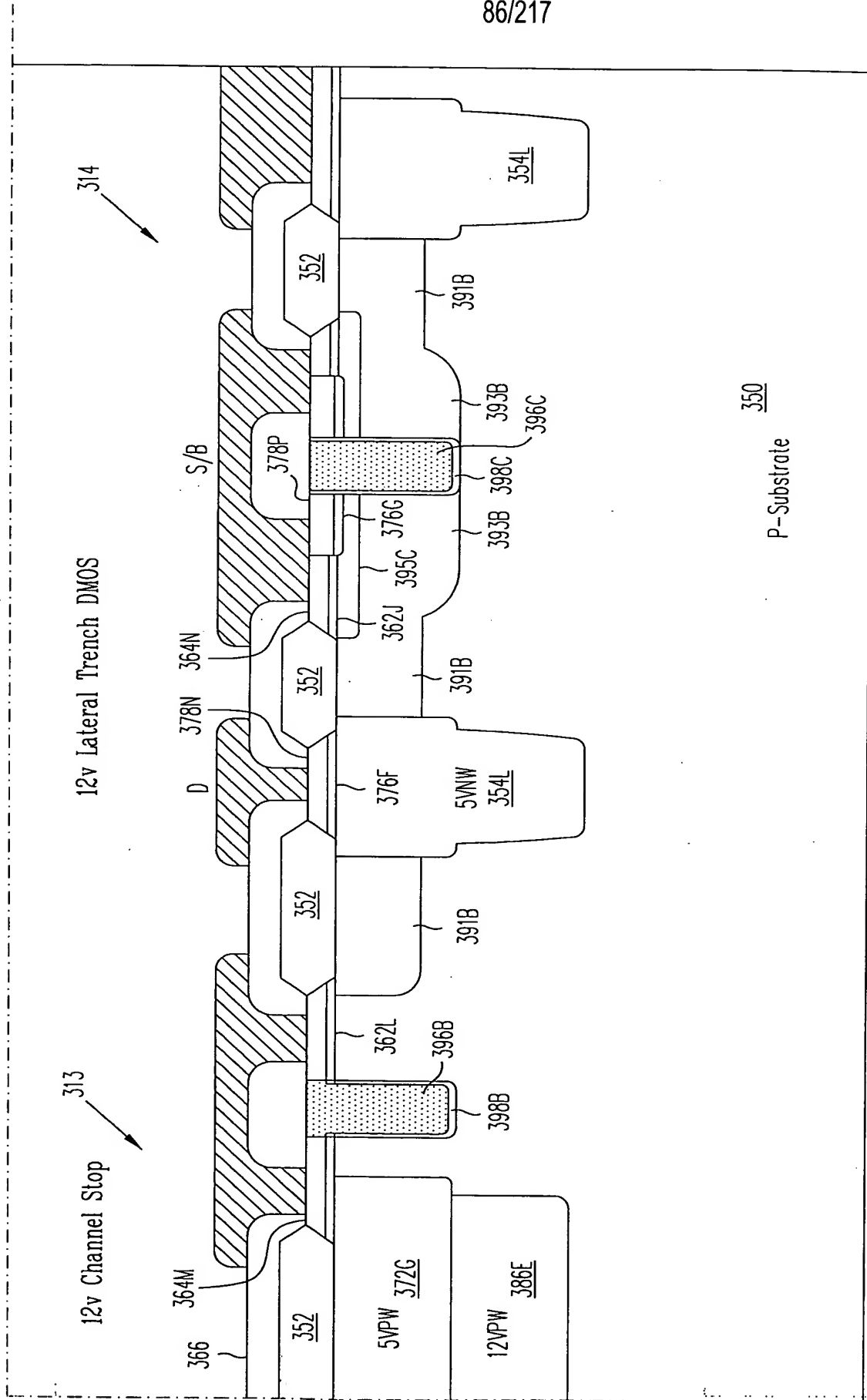


FIG. 18B-4

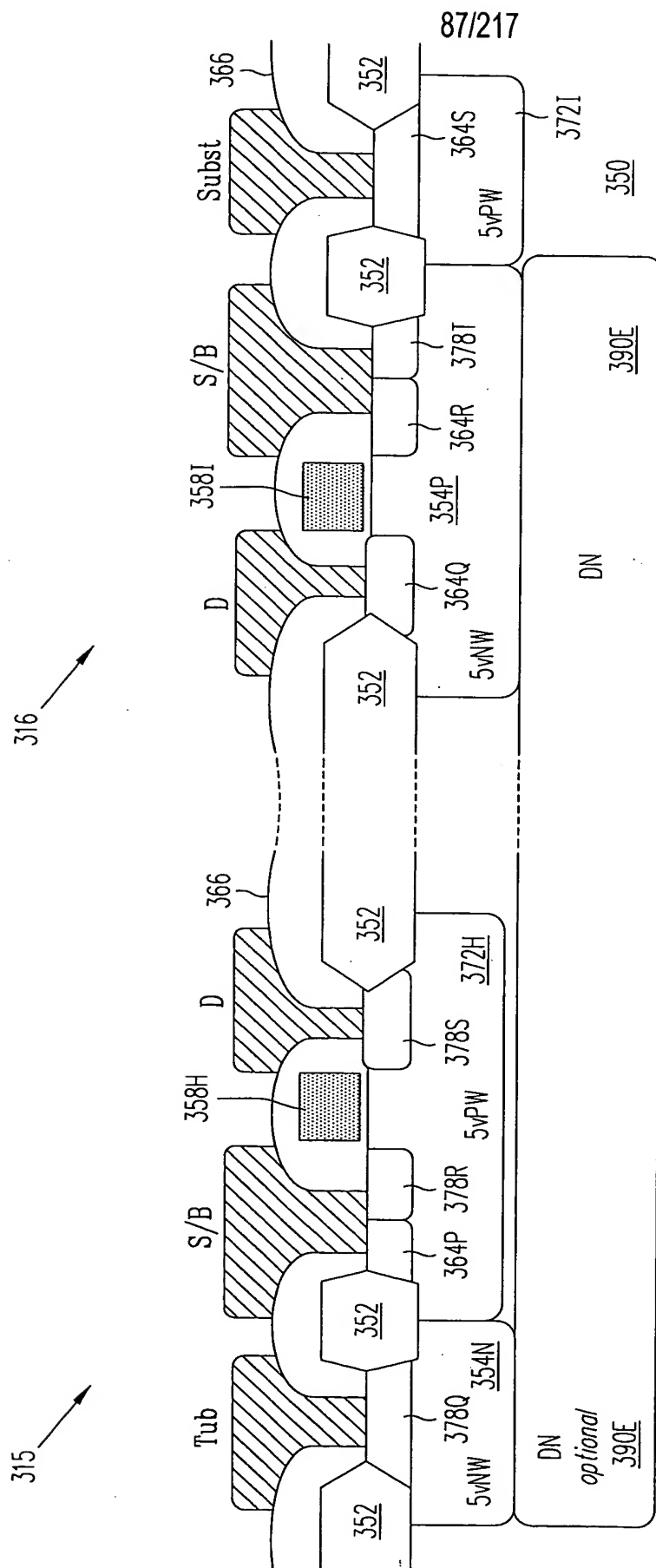


FIG. 18C

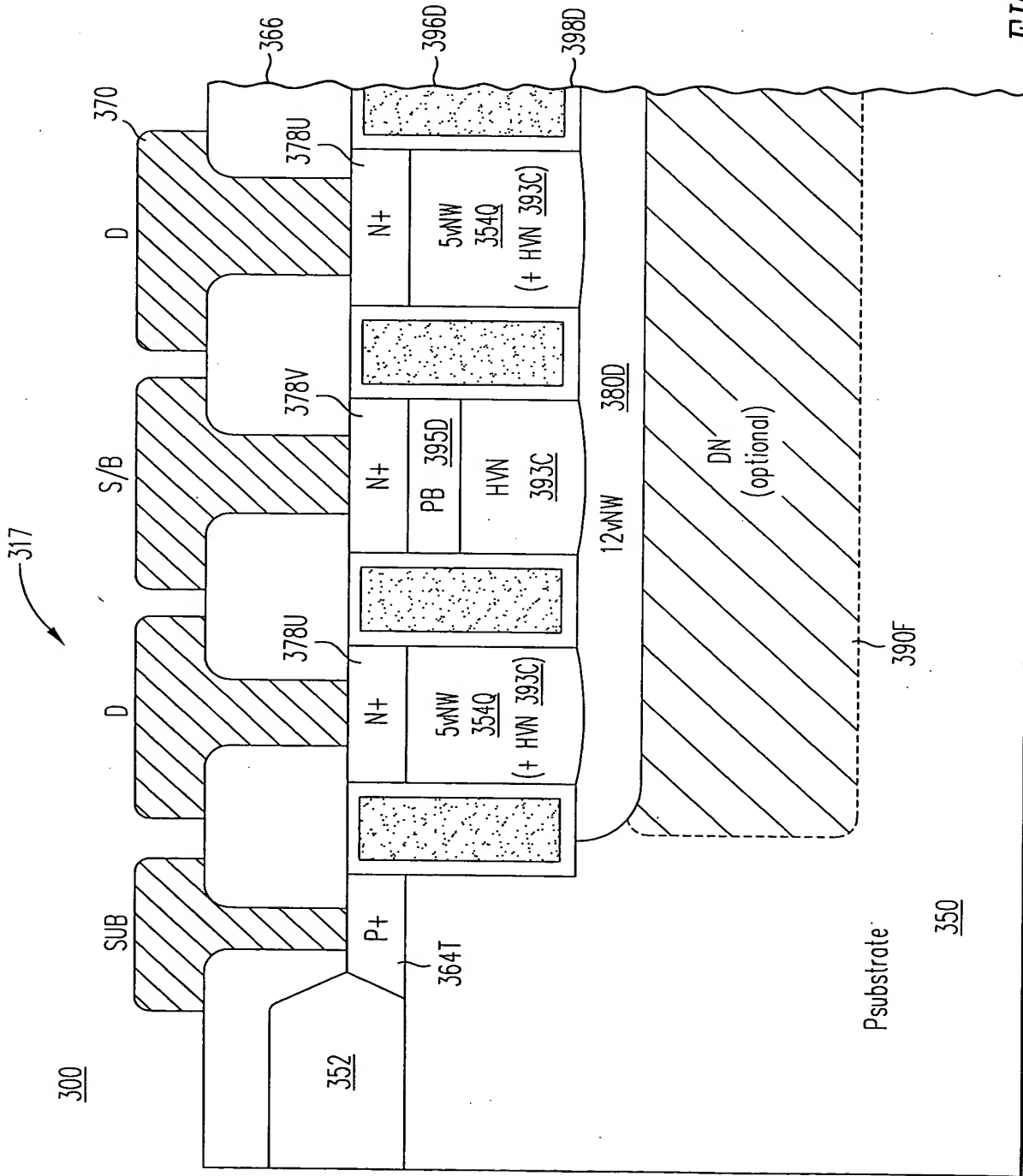
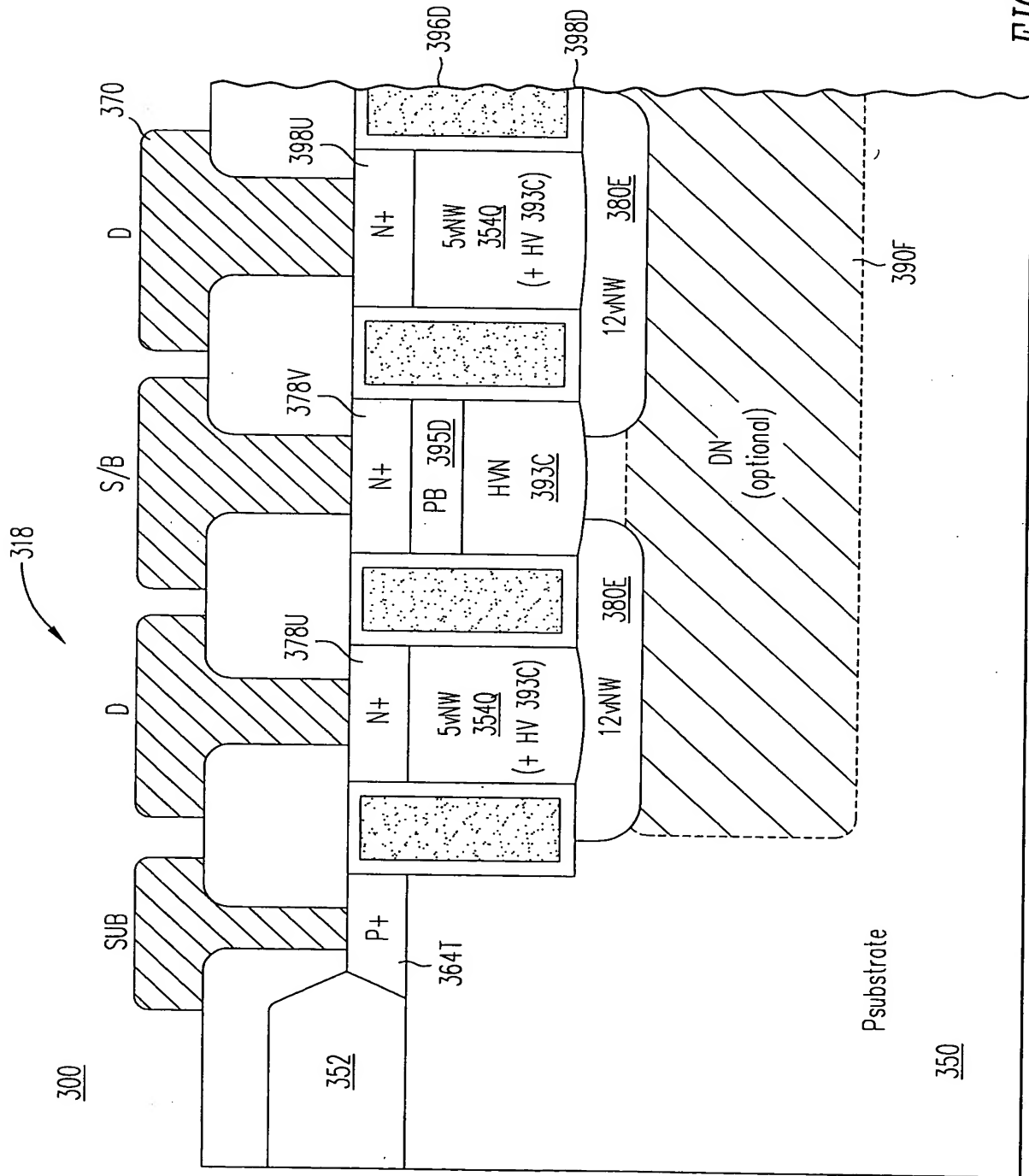


FIG. 18D



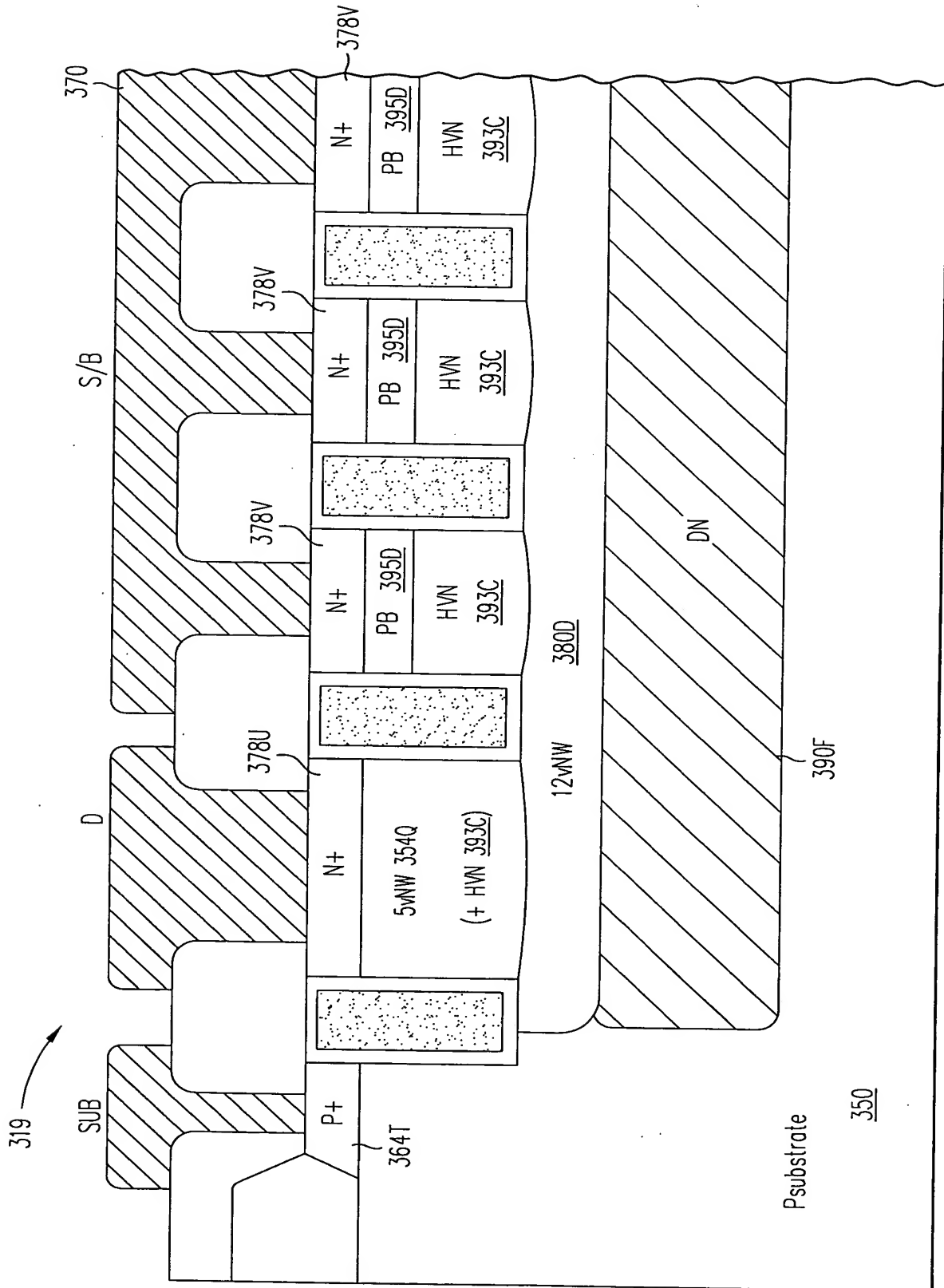


FIG. 18F

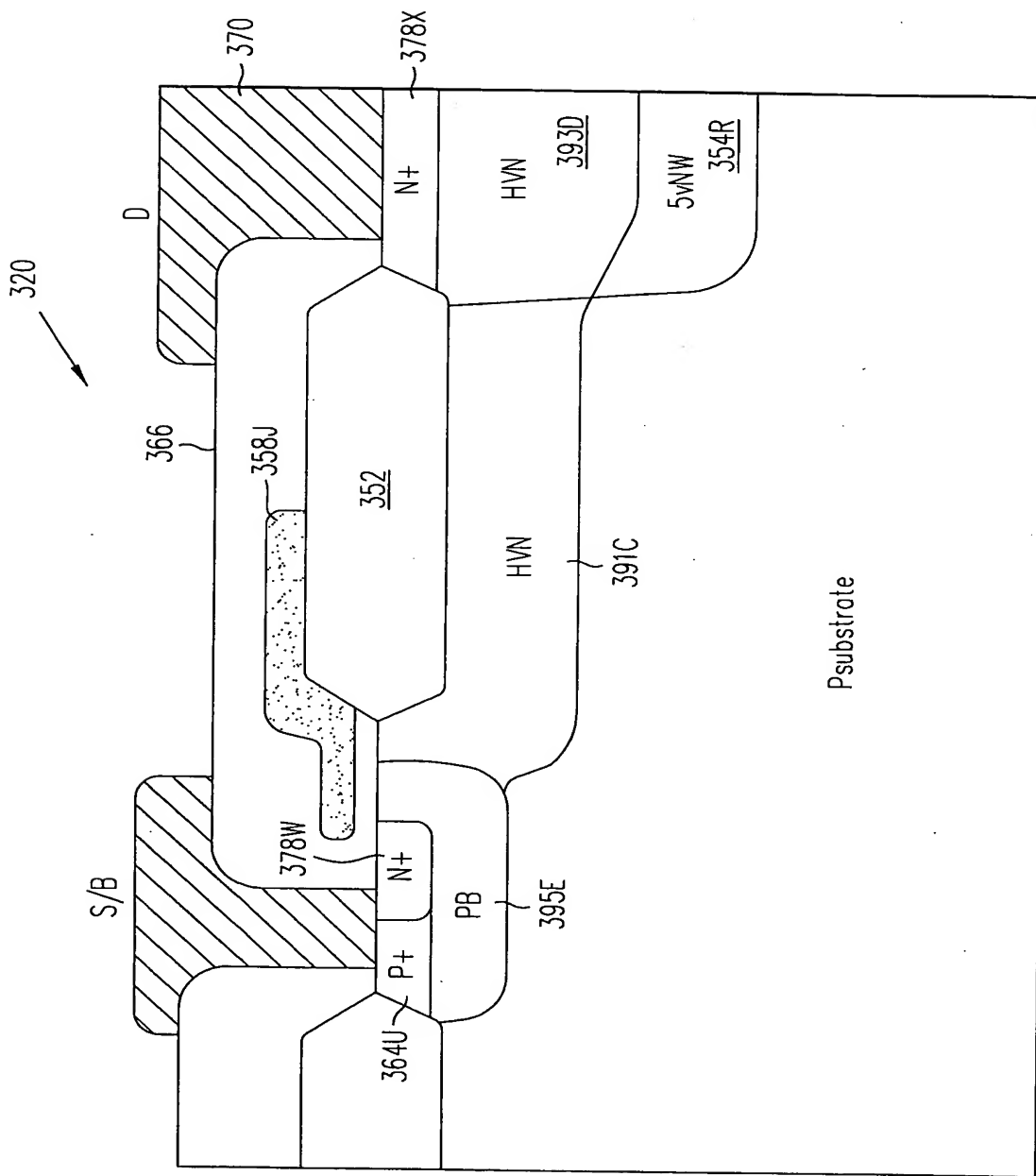


FIG. 18G

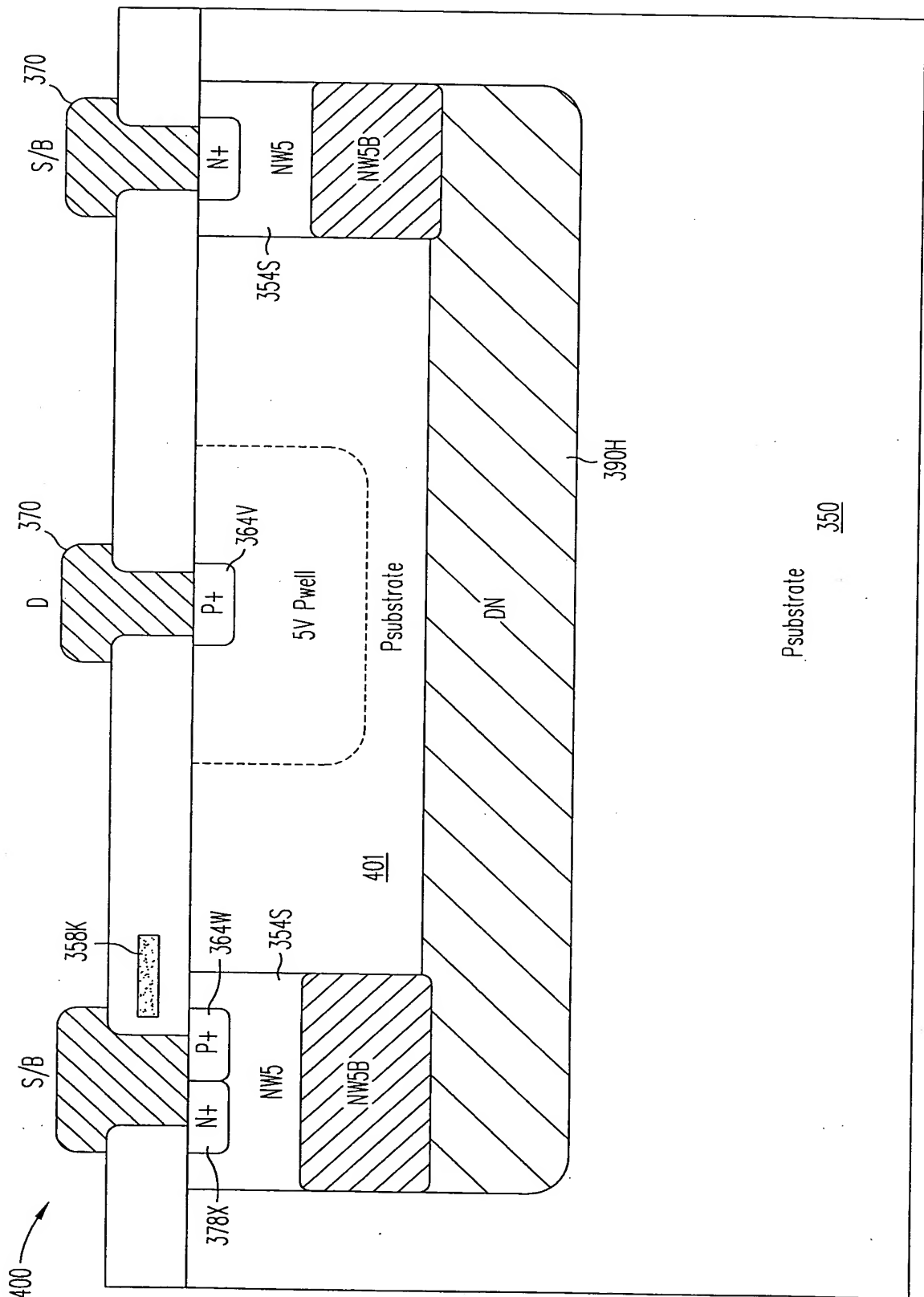
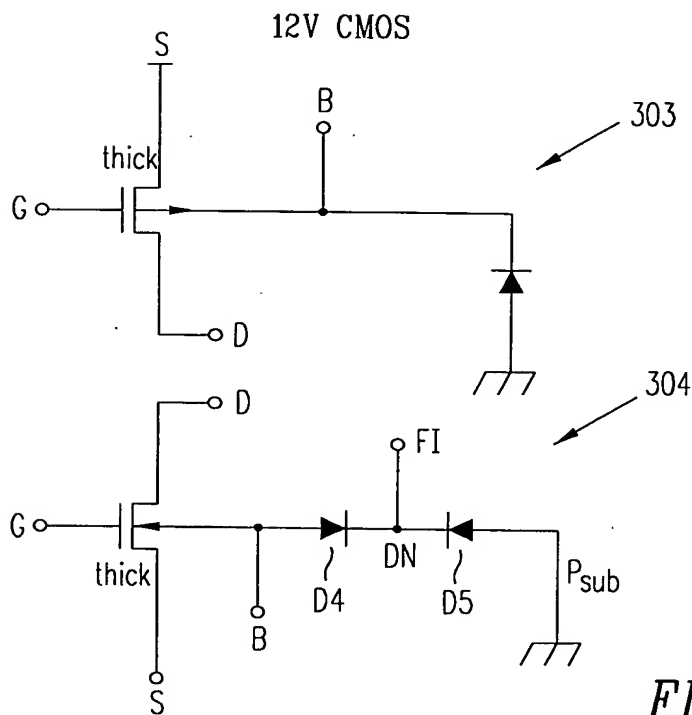
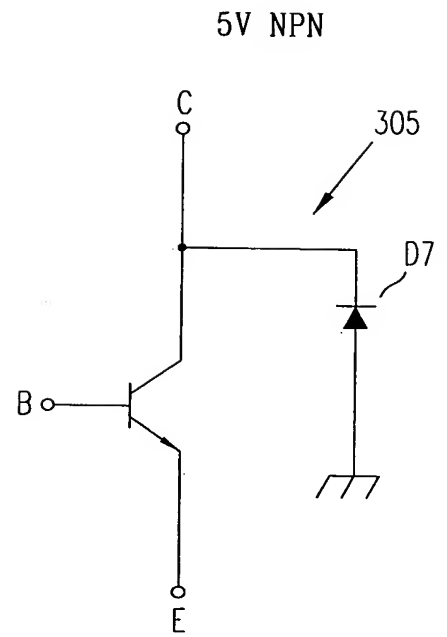
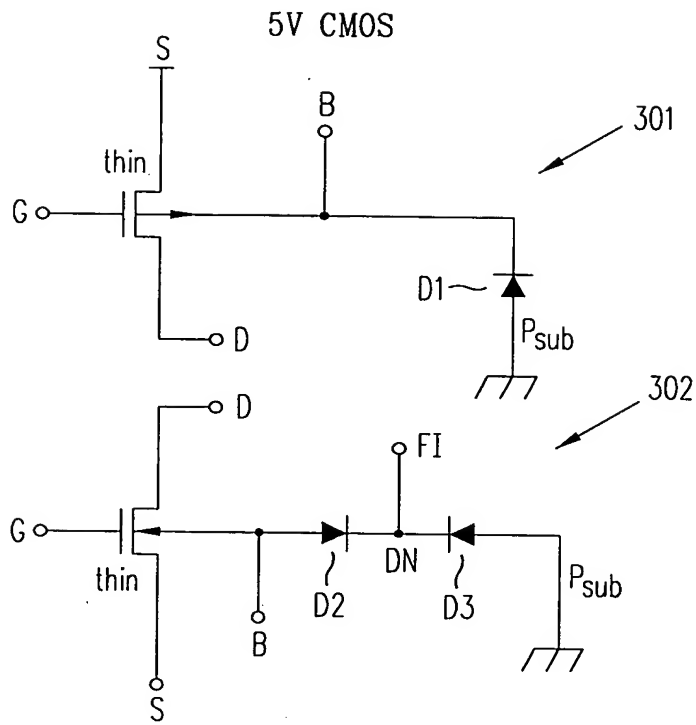


FIG. 18H



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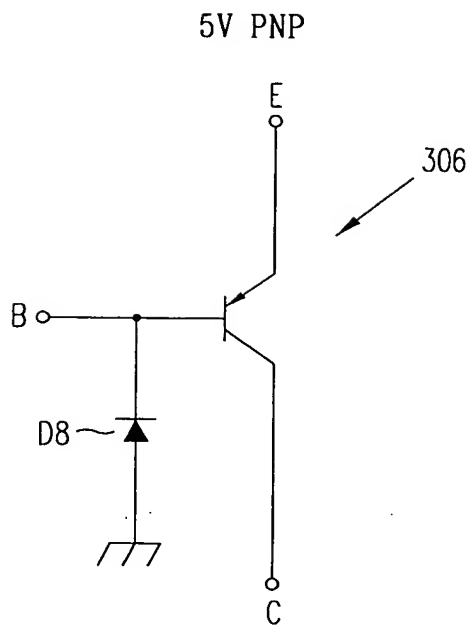


FIG. 19D

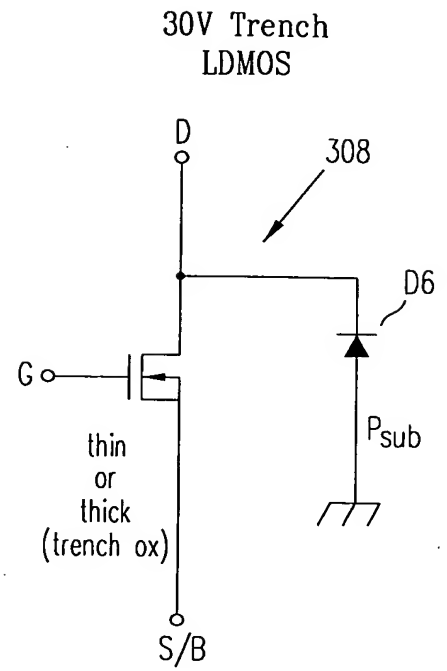


FIG. 19E

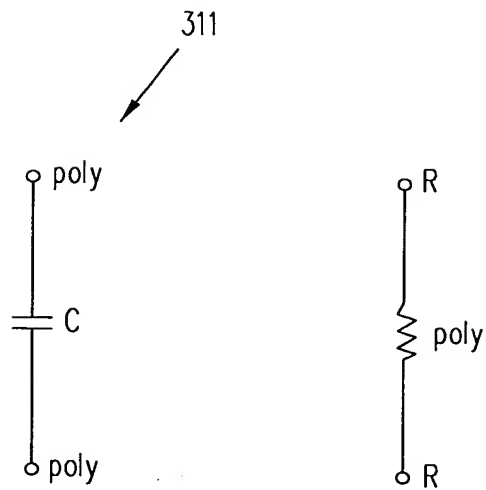


FIG. 19F

FIG. 19G

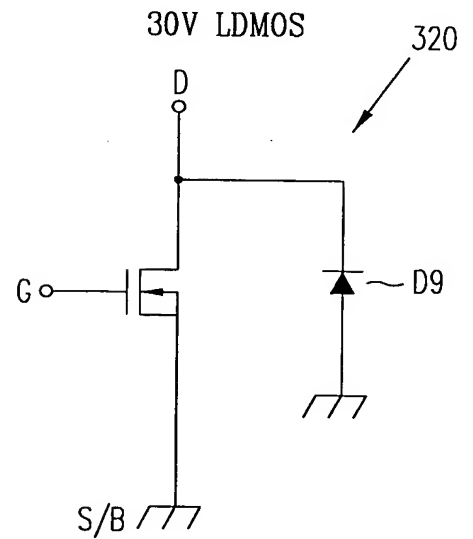
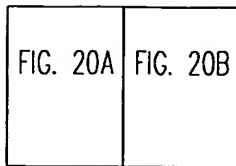
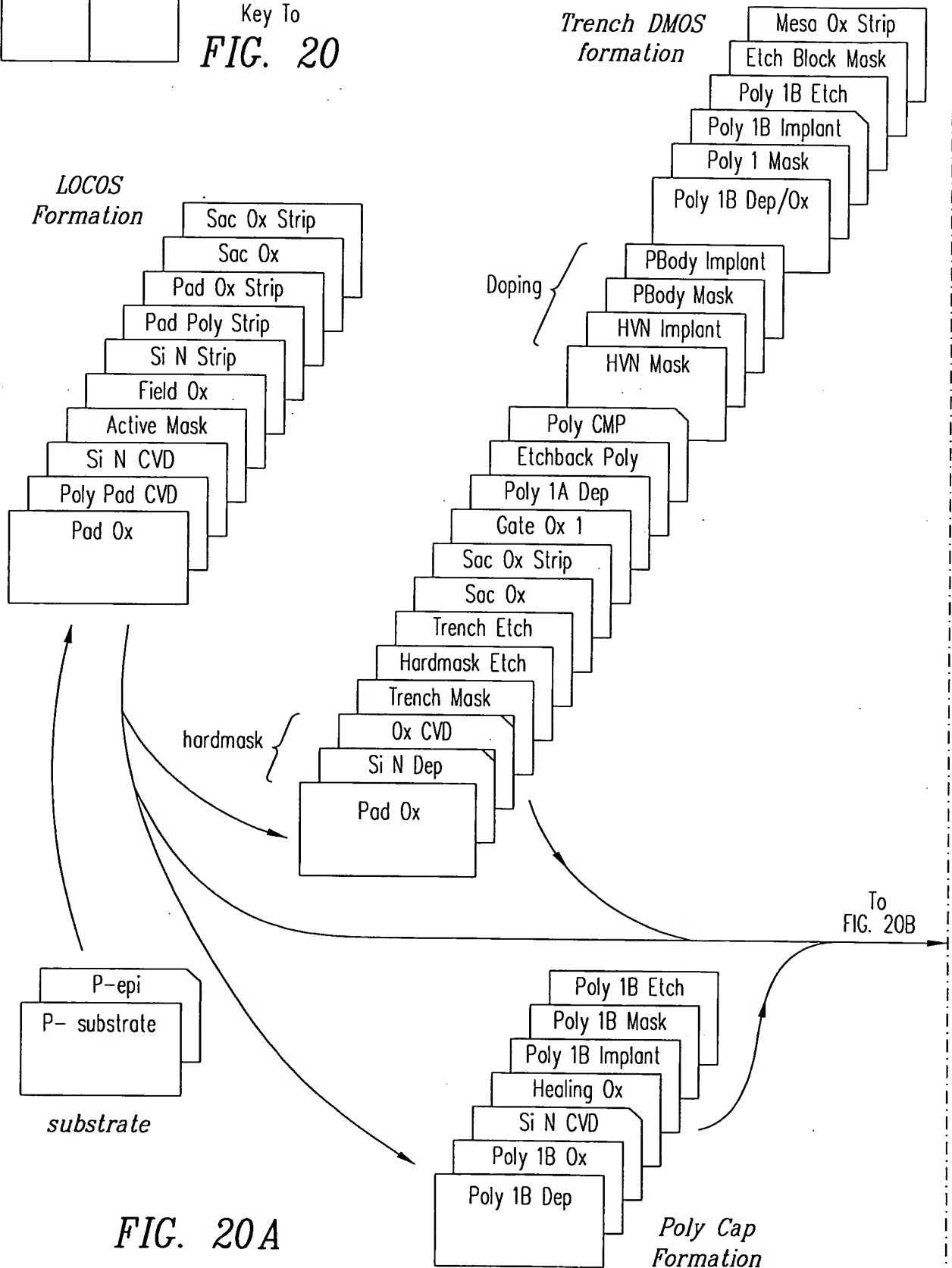


FIG. 19H



Key To  
**FIG. 20**



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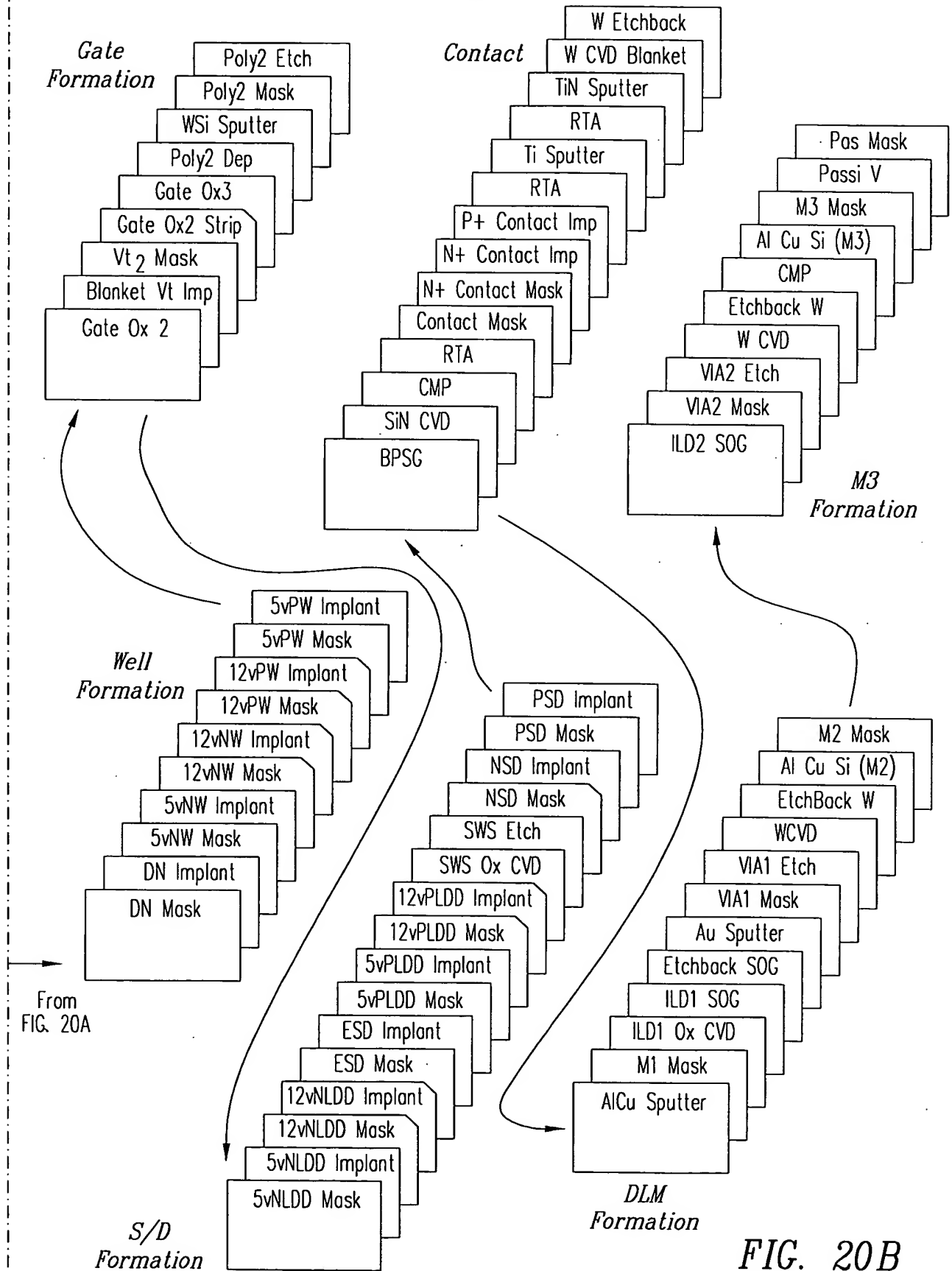


FIG. 20B

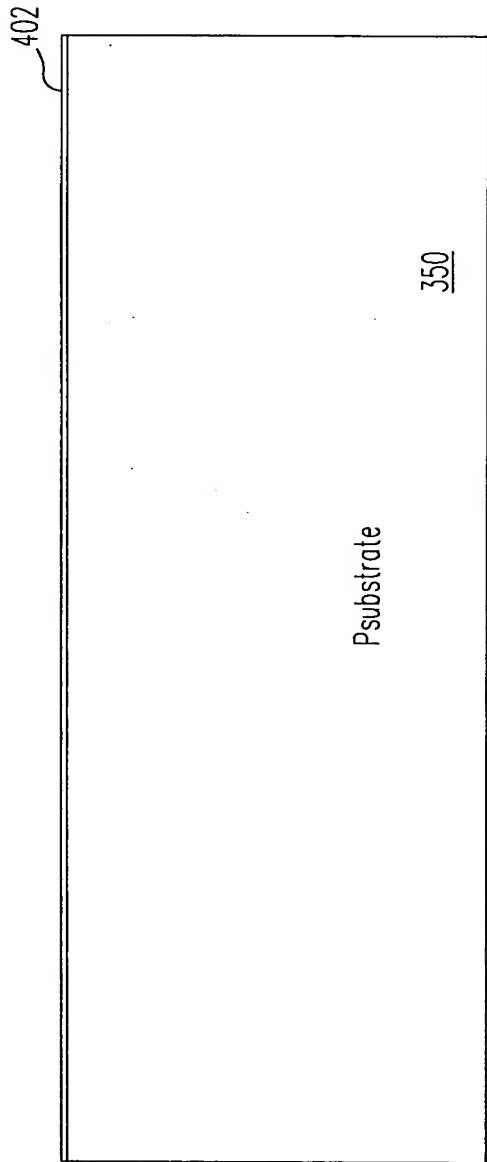


FIG. 21

First Pad Oxide Layer

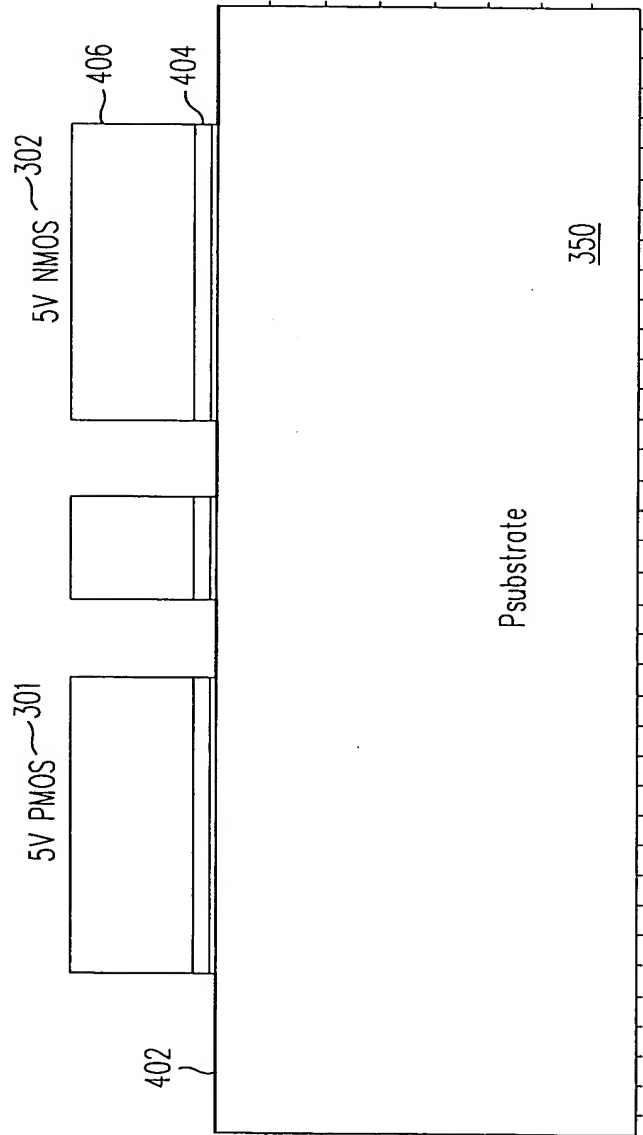


FIG. 22A

LOCOS-Nitride Mask and Etch

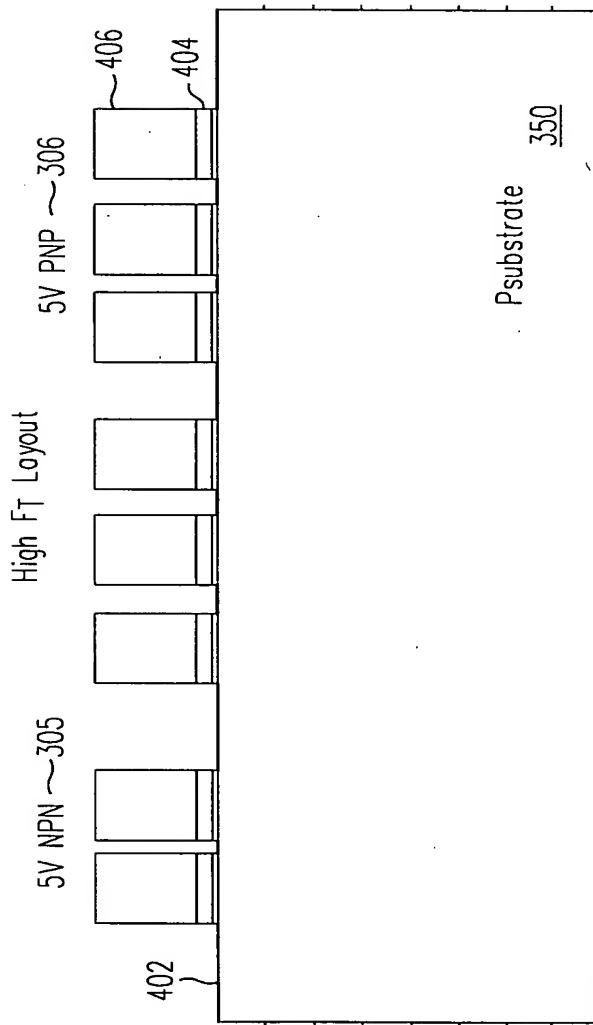


FIG. 22B

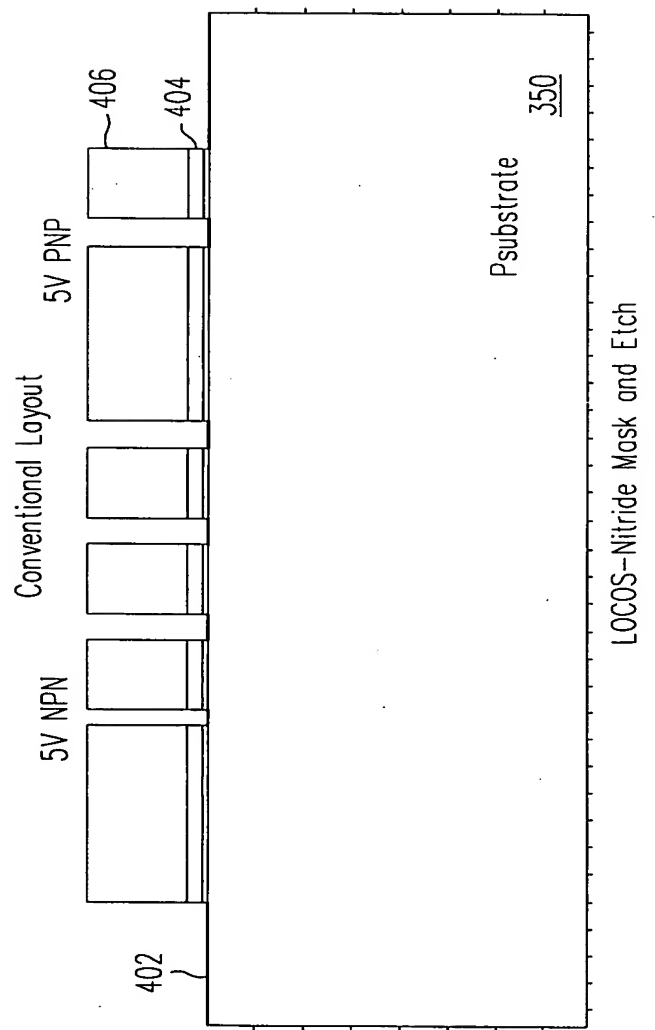


FIG. 22C

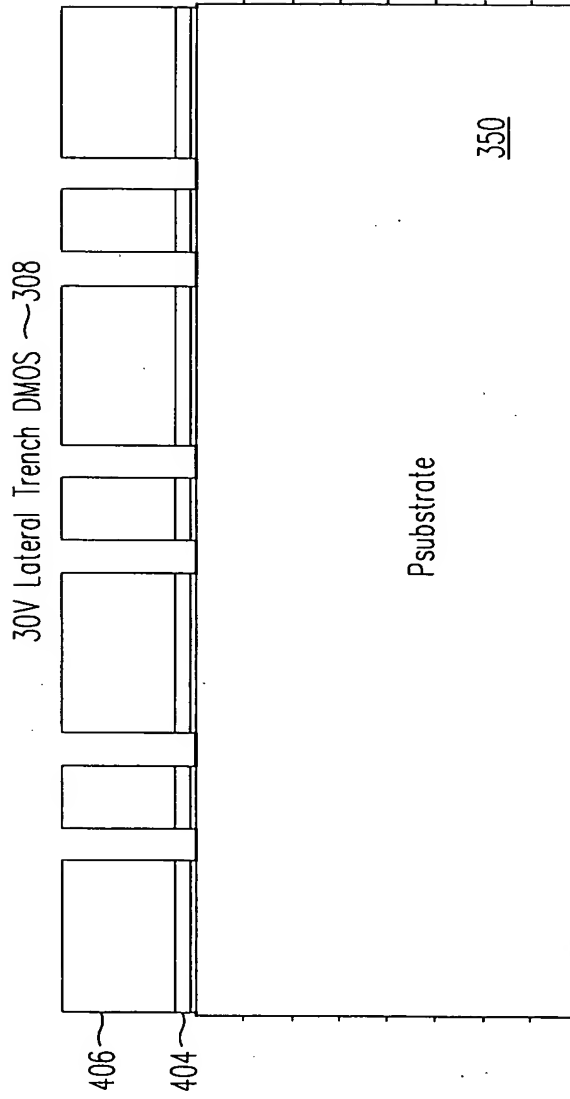


FIG. 22D

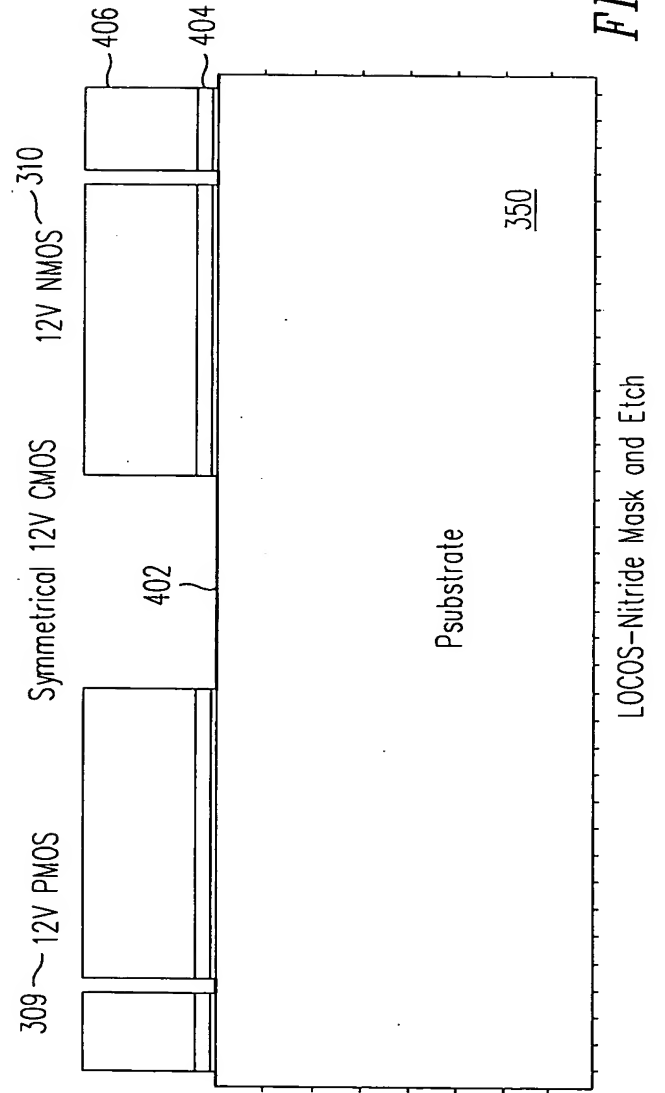


FIG. 22E

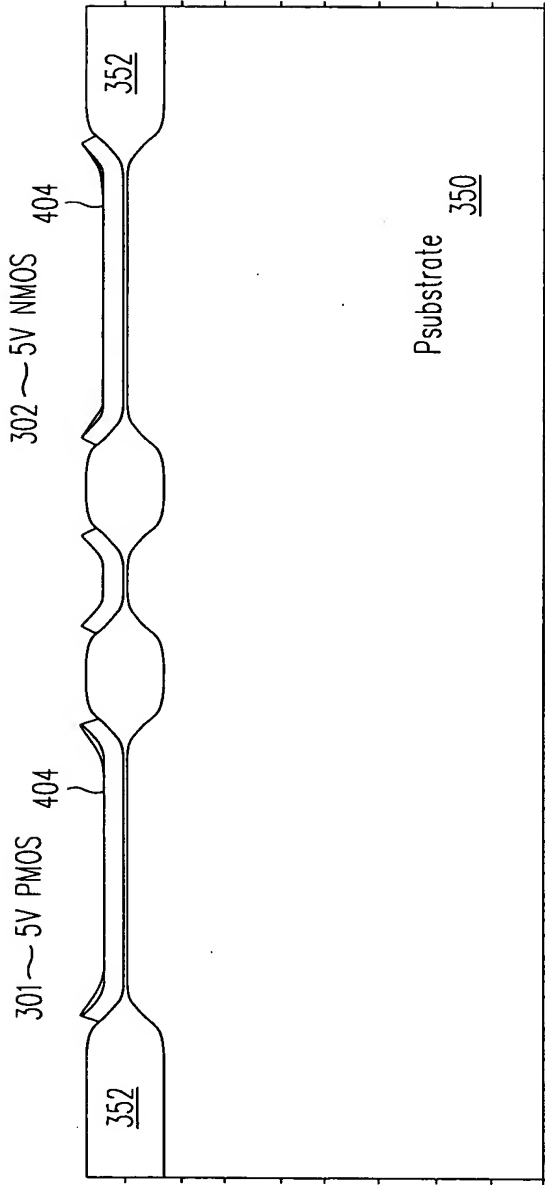


FIG. 23A

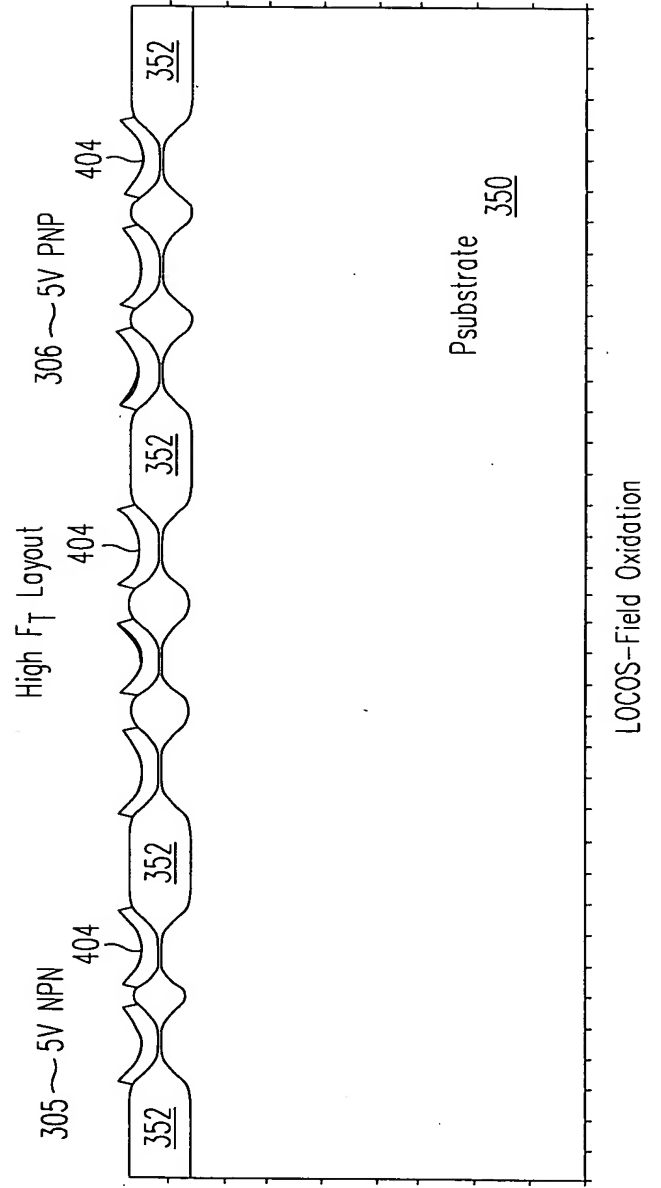


FIG. 23B



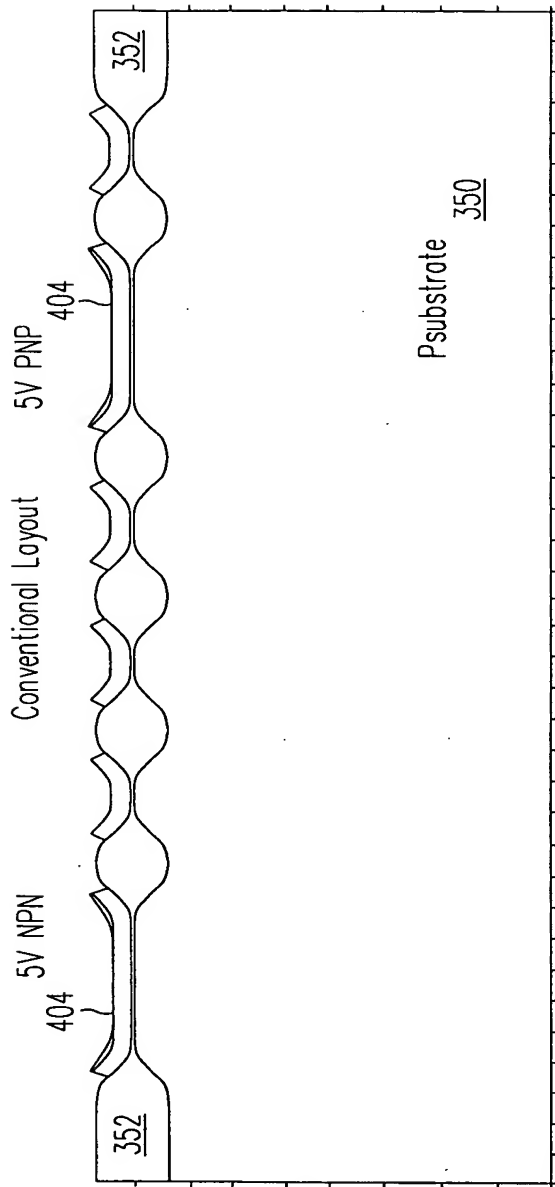


FIG. 23C

LOCOS-Field Oxidation

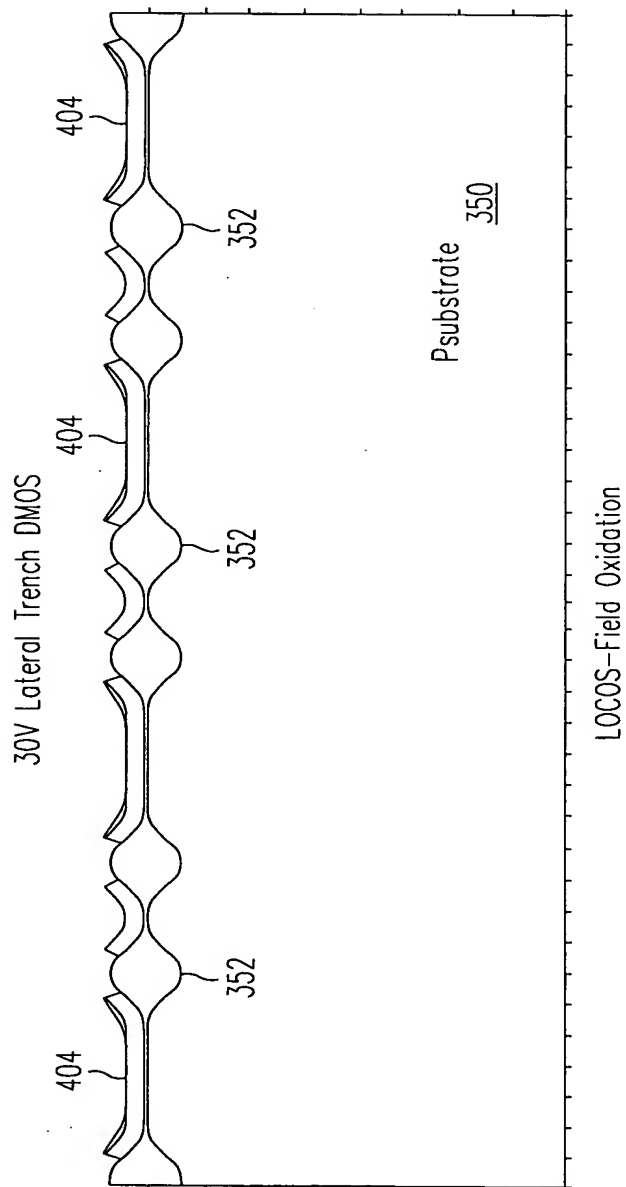


FIG. 23D

LOCOS-Field Oxidation

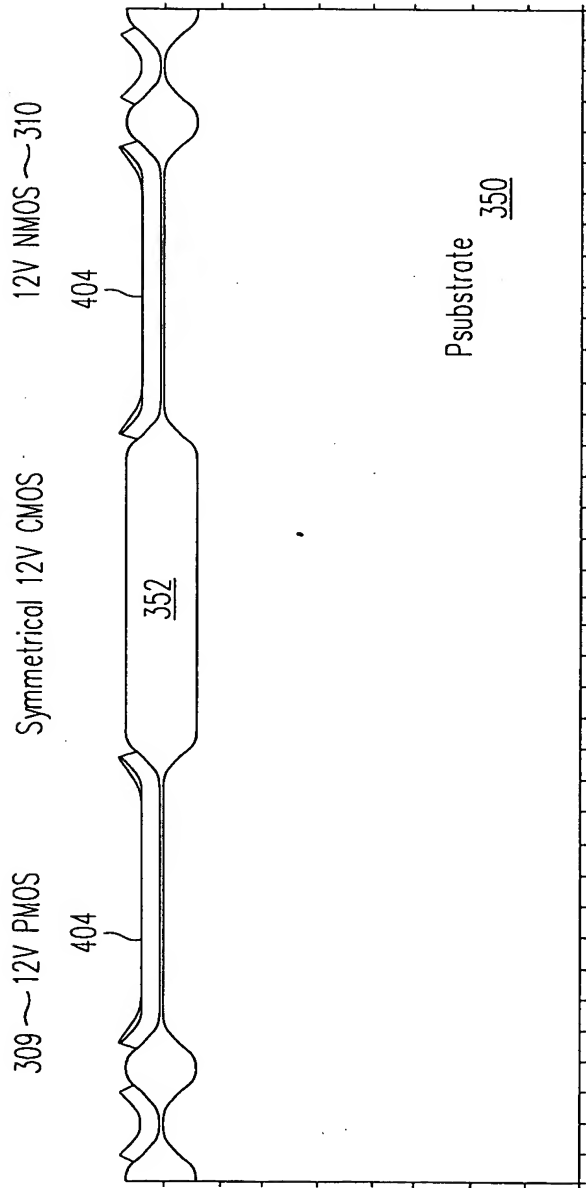


FIG. 23E

LOCOS-Field Oxidation

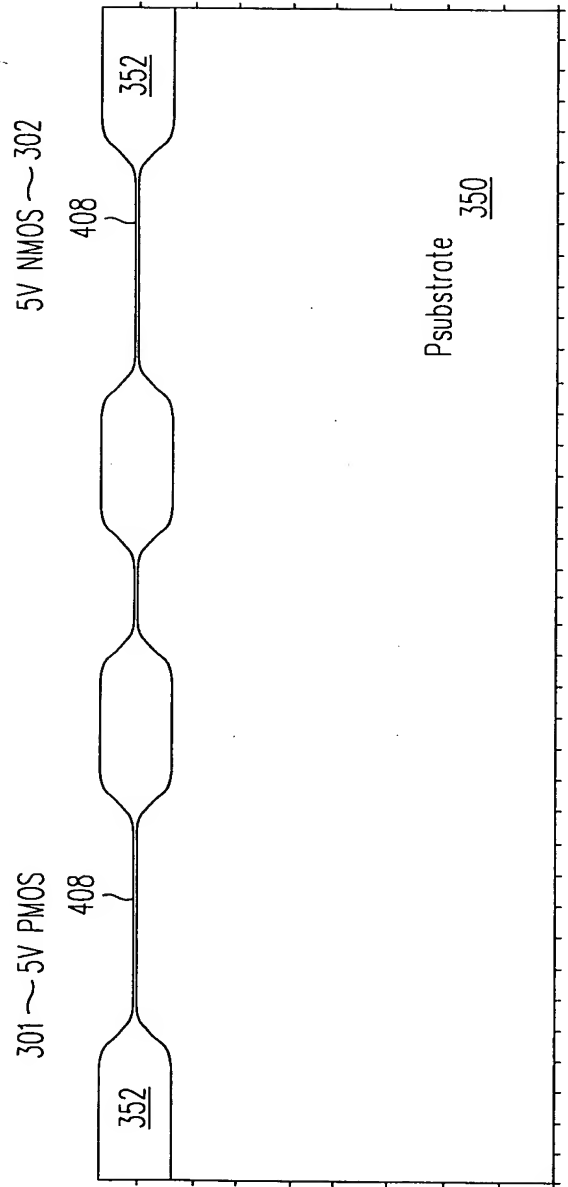


FIG. 24A

Second Pad Oxide Layer

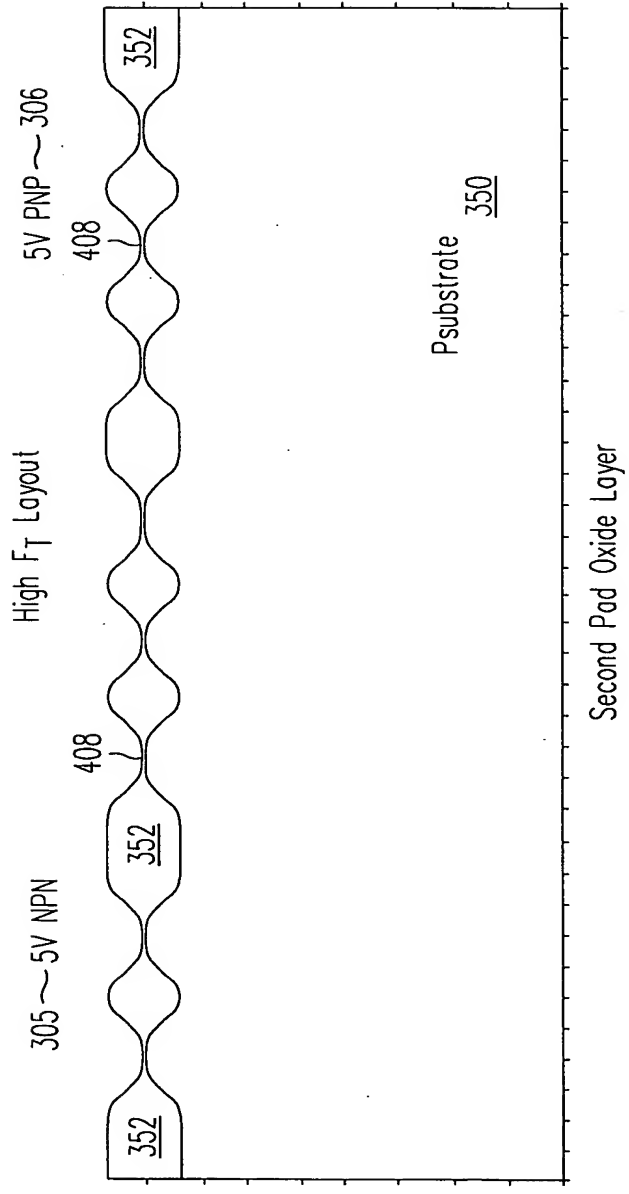


FIG. 24B

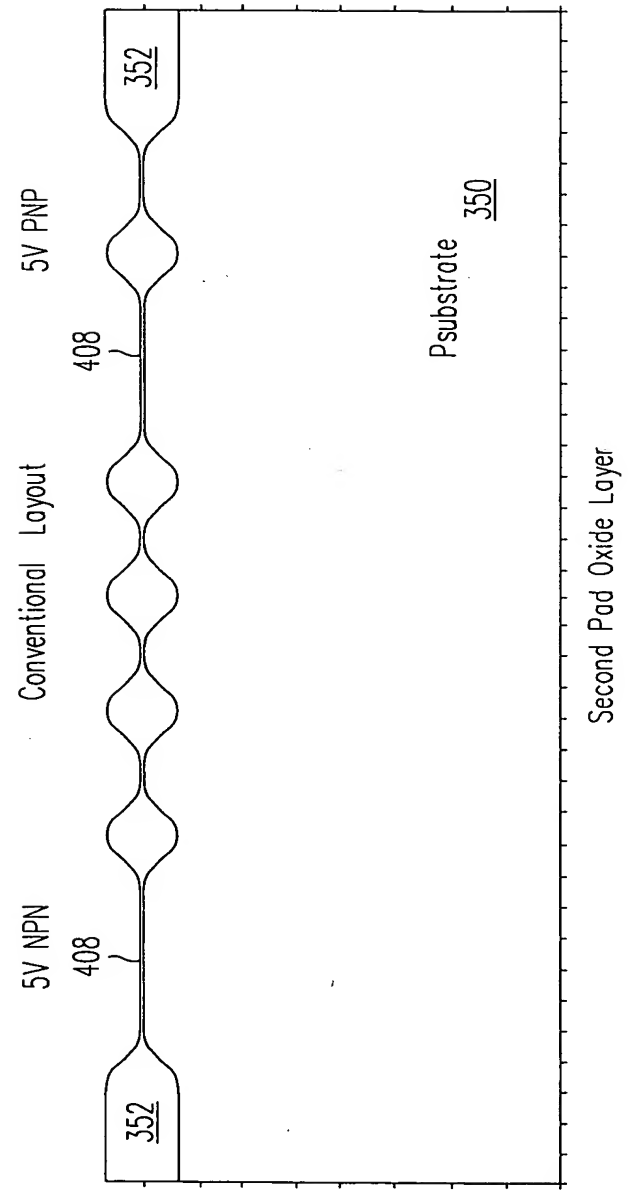
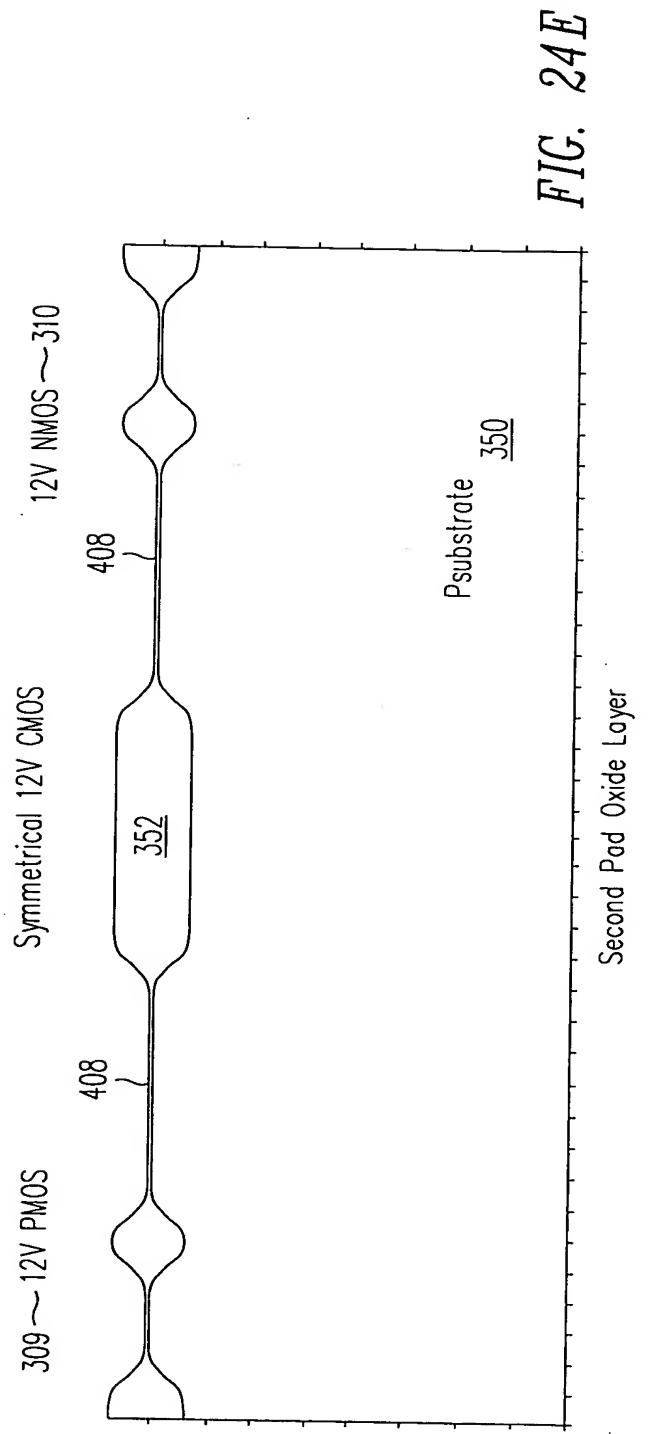
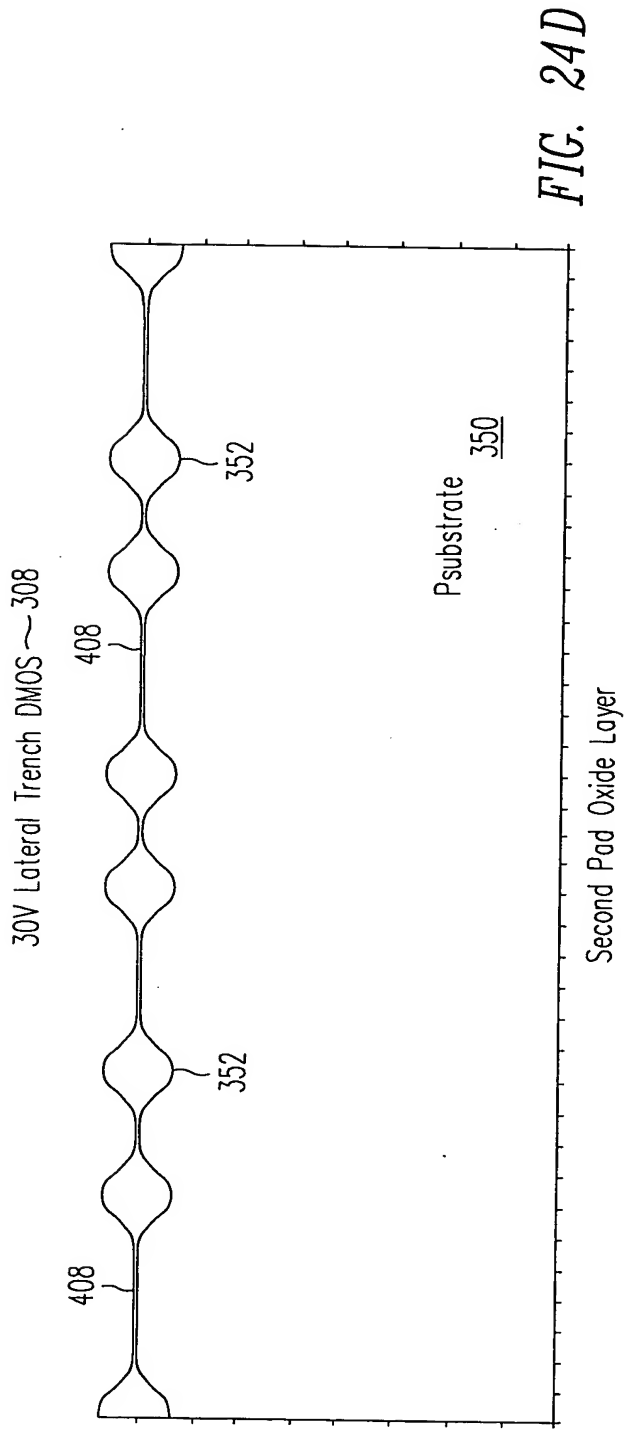
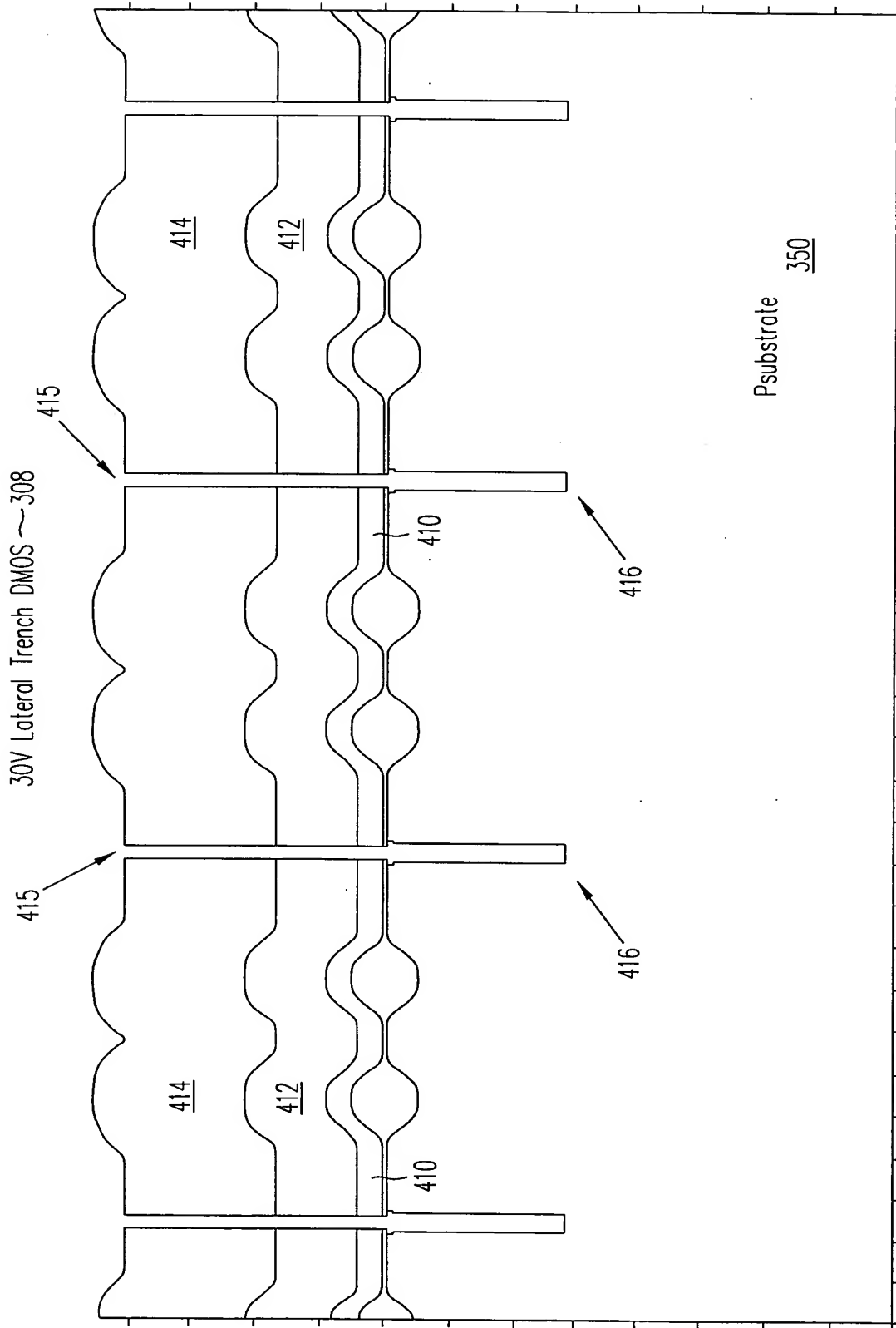


FIG. 24C

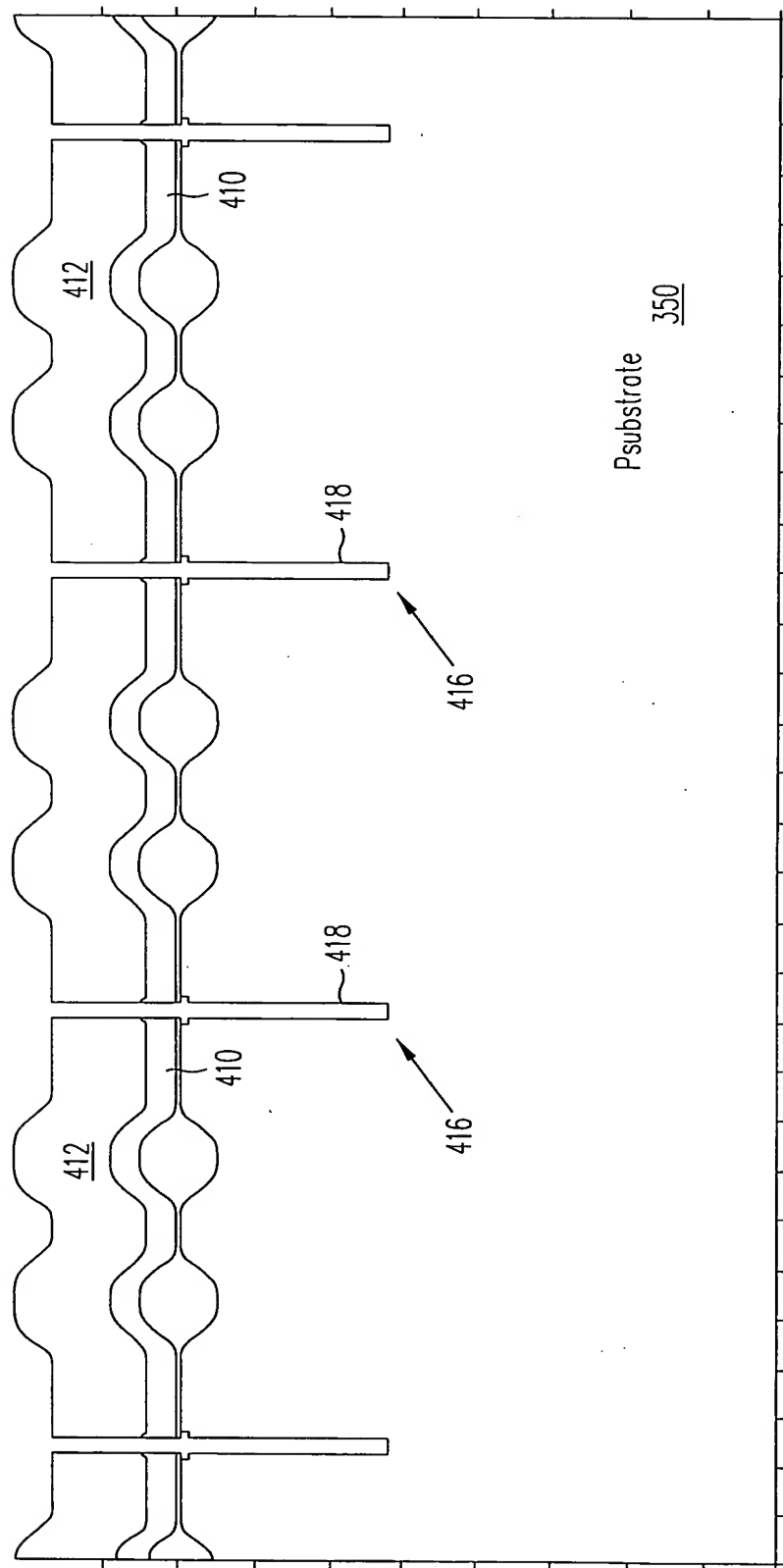




Trench Hard Mask

FIG. 25D

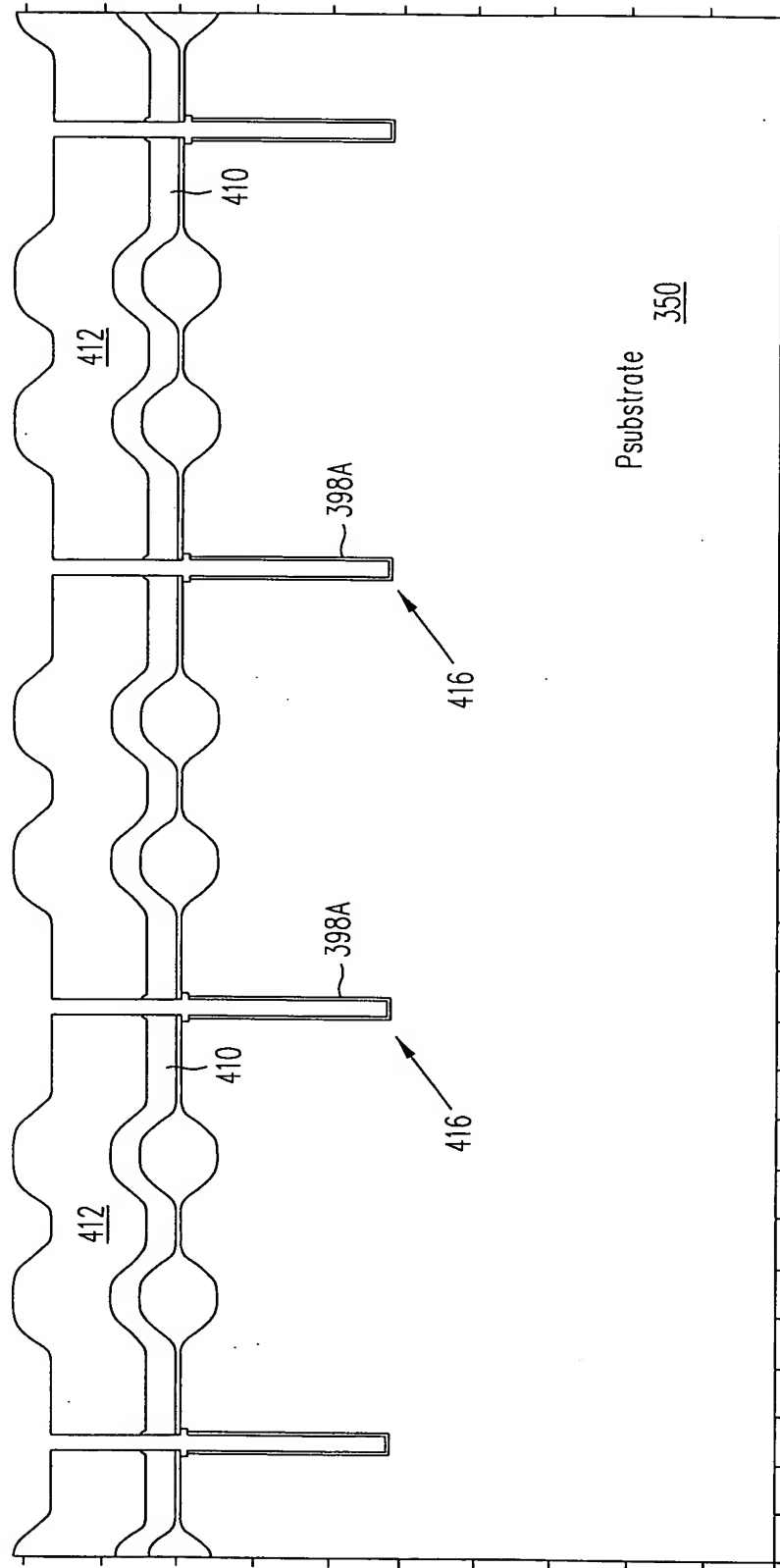
30V Lateral Trench DMOS ~ 308



Sacrificial Oxide

FIG. 26D

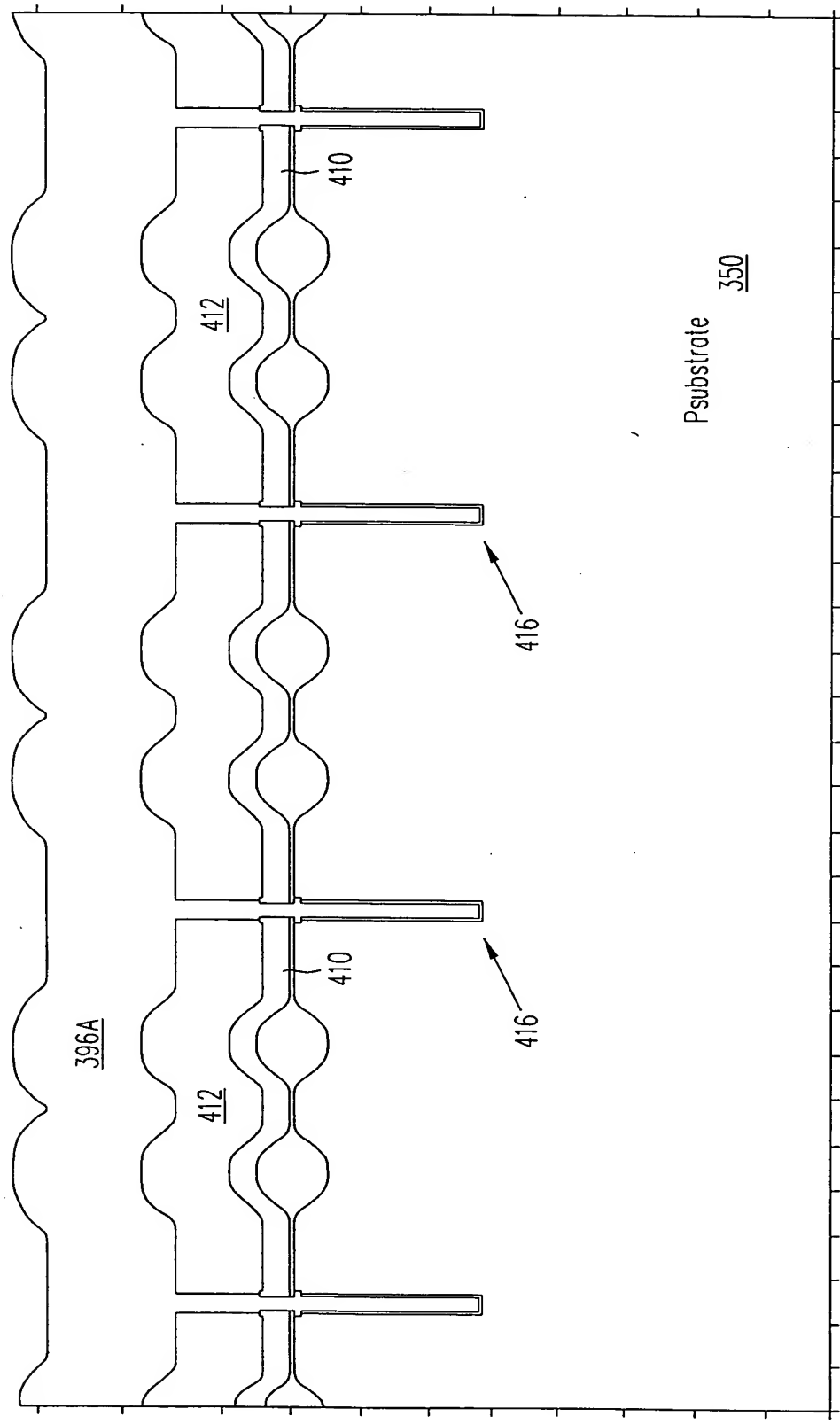
30V Lateral Trench DMOS ~ 308



Trench Gate Oxide

FIG. 27D

30V Lateral Trench DMOS ~308

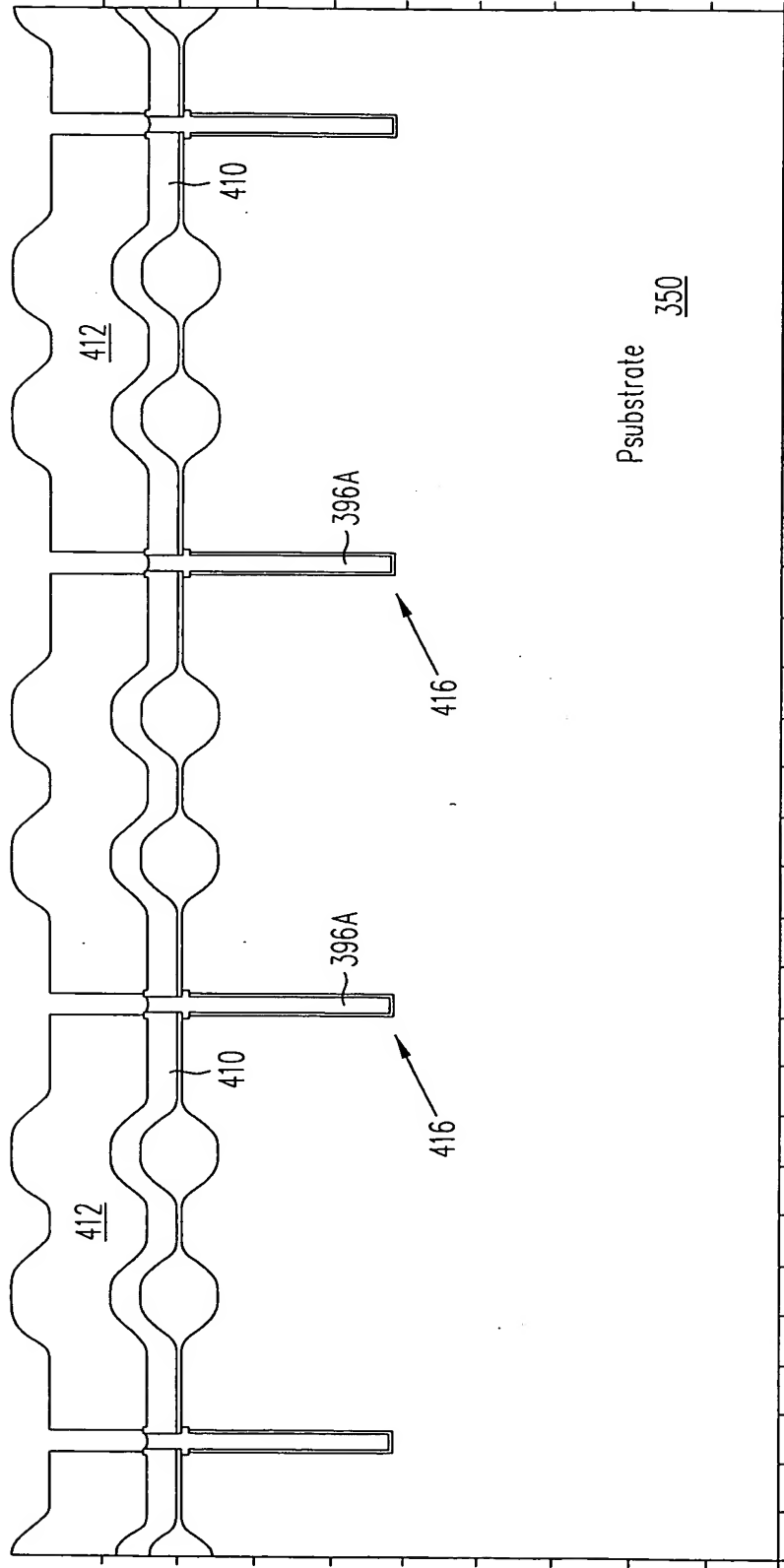


Polysilicon-First Layer

FIG. 28D



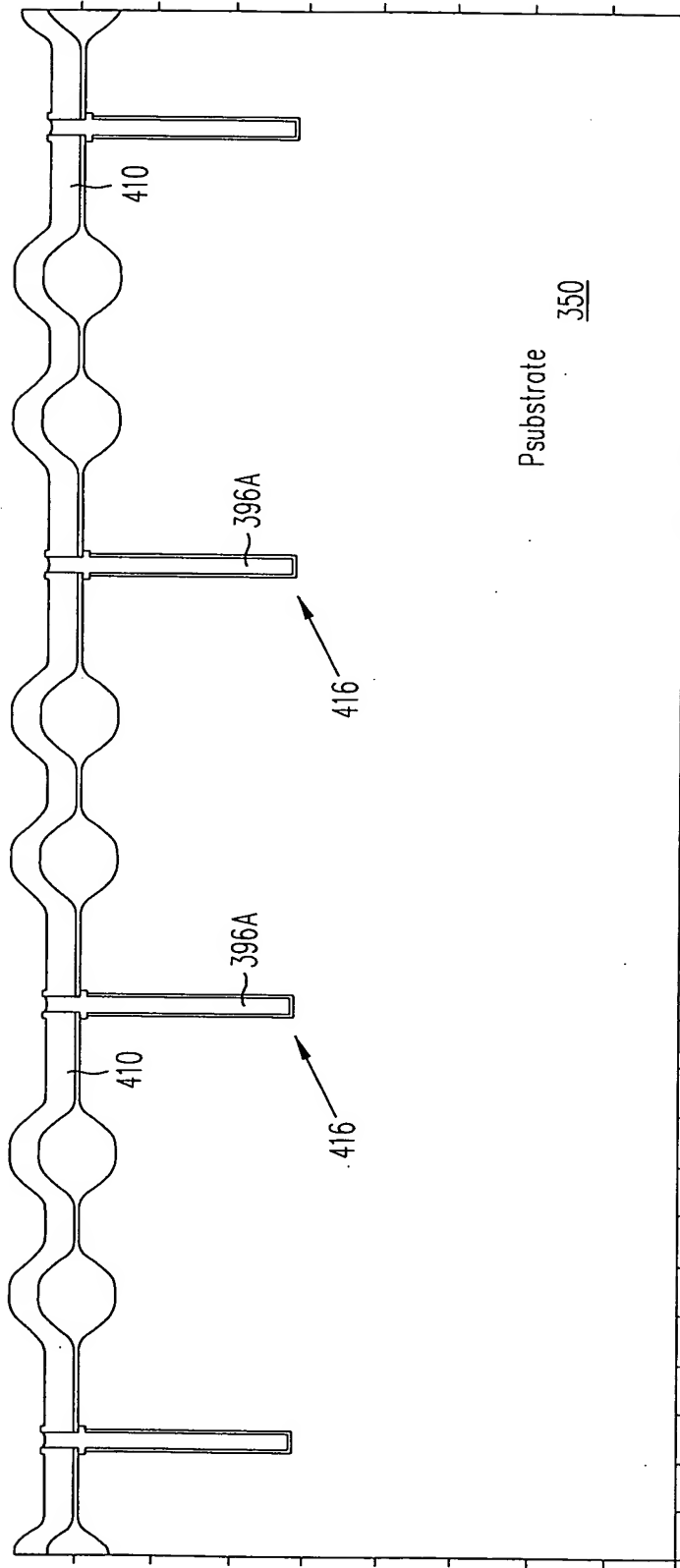
30V Lateral Trench DMOS ~ 308



Polysilicon Etchback-First Layer

FIG. 29D

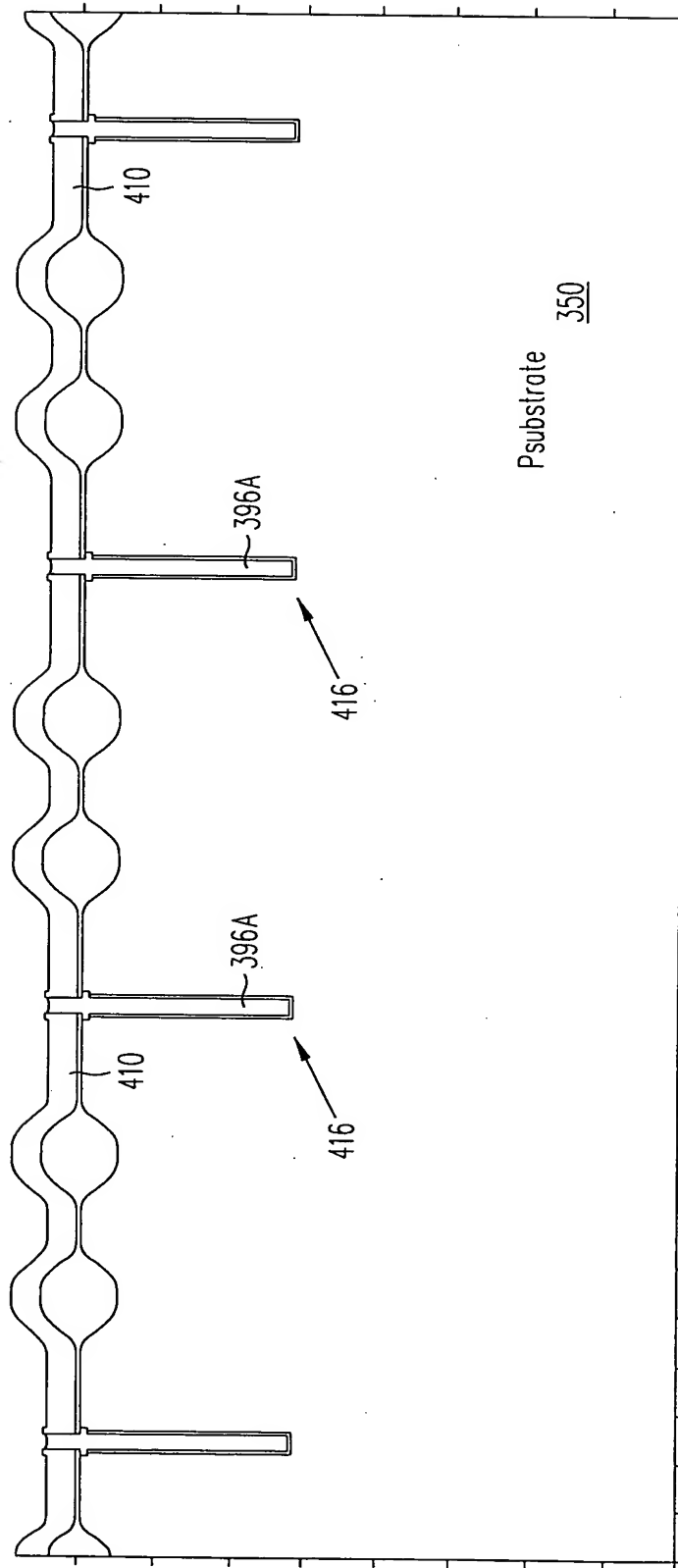
30V Lateral Trench DMOS ~ 308



Hard Mask Removal

*FIG. 30D*

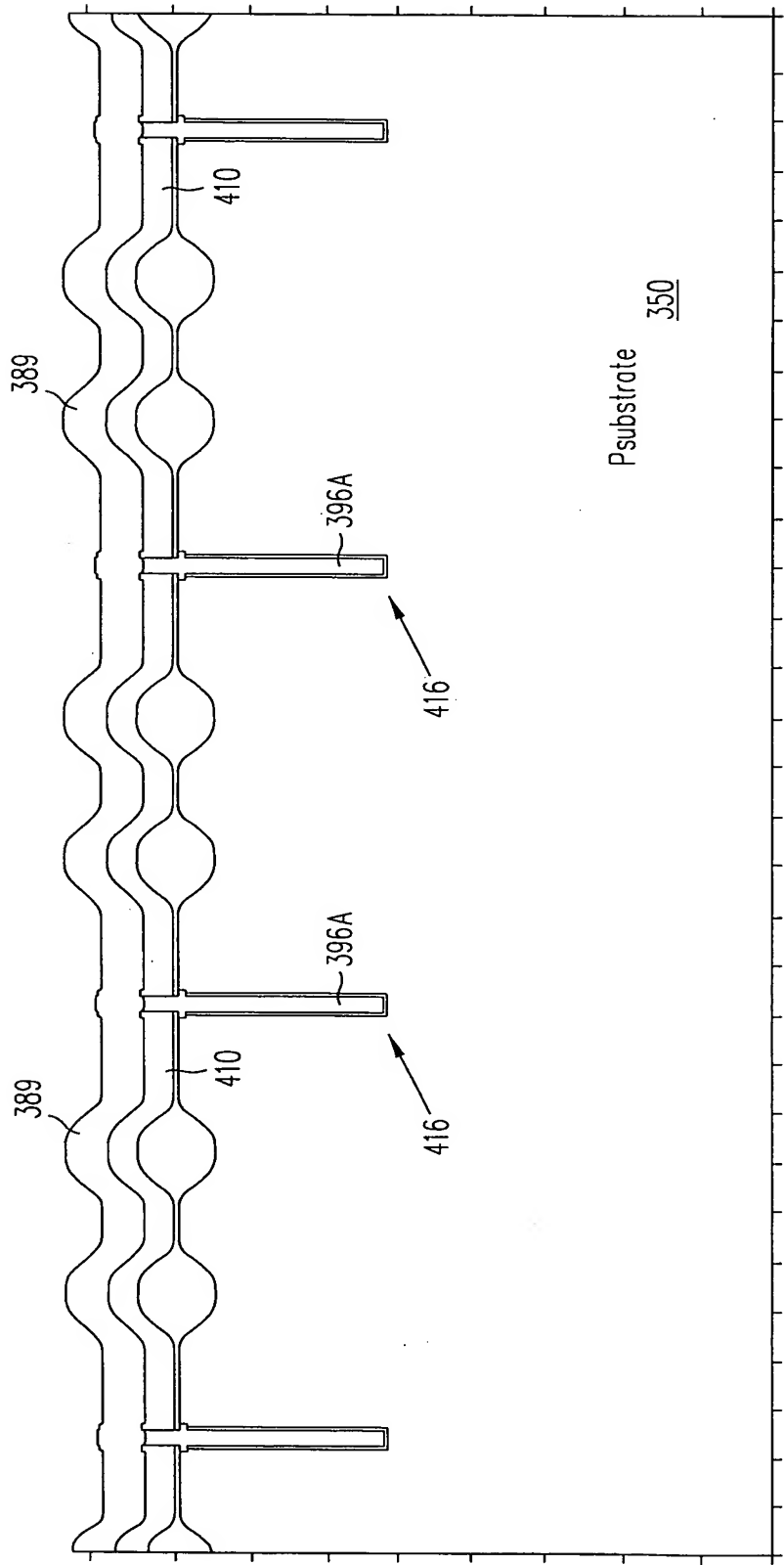
30V Lateral Trench DMOS ~ 308



Second Polysilicon Etchback-First Layer

FIG. 31D

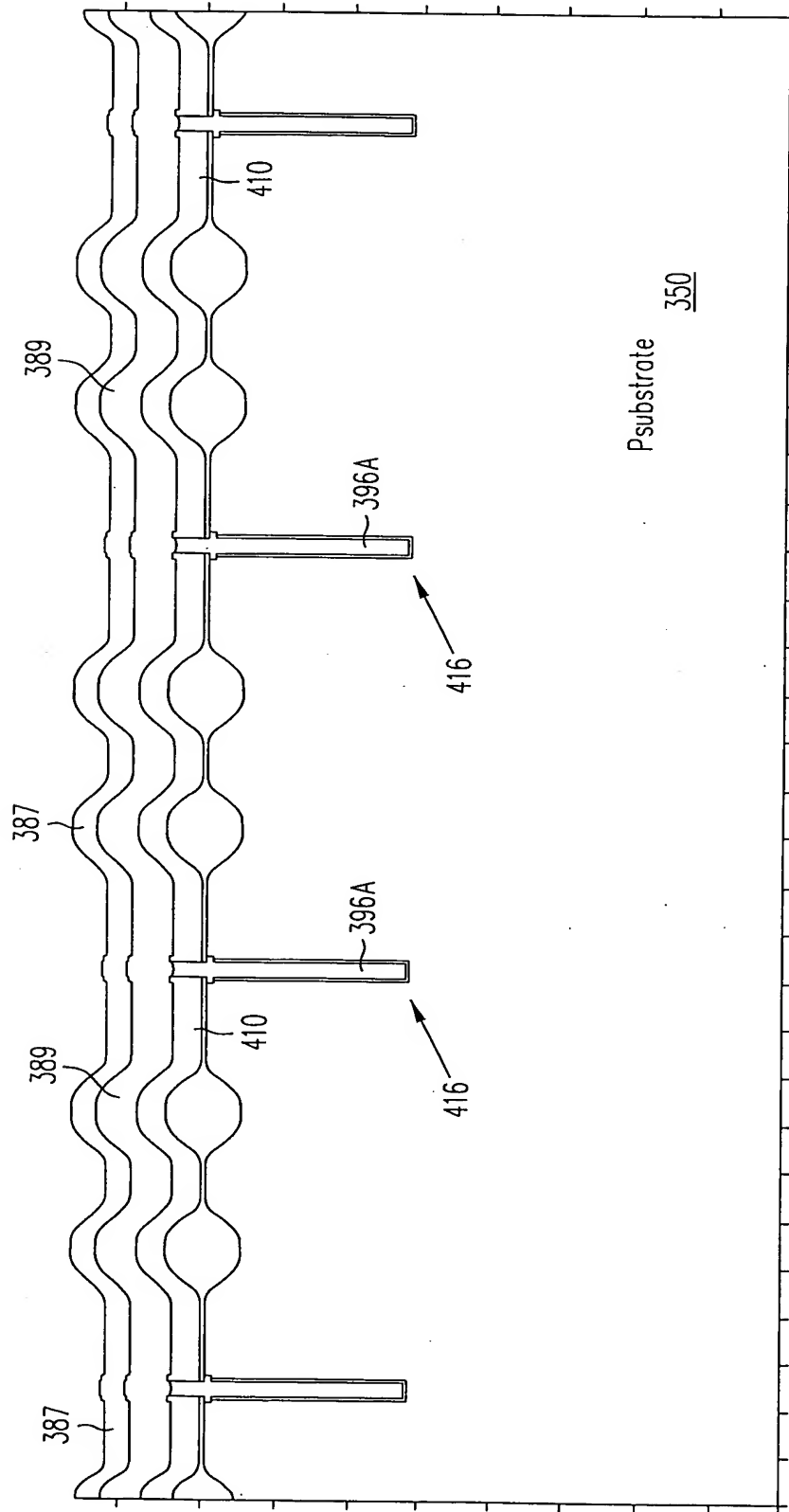
30V Lateral Trench DMOS ~308



Polysilicon-Second Layer

FIG. 32D

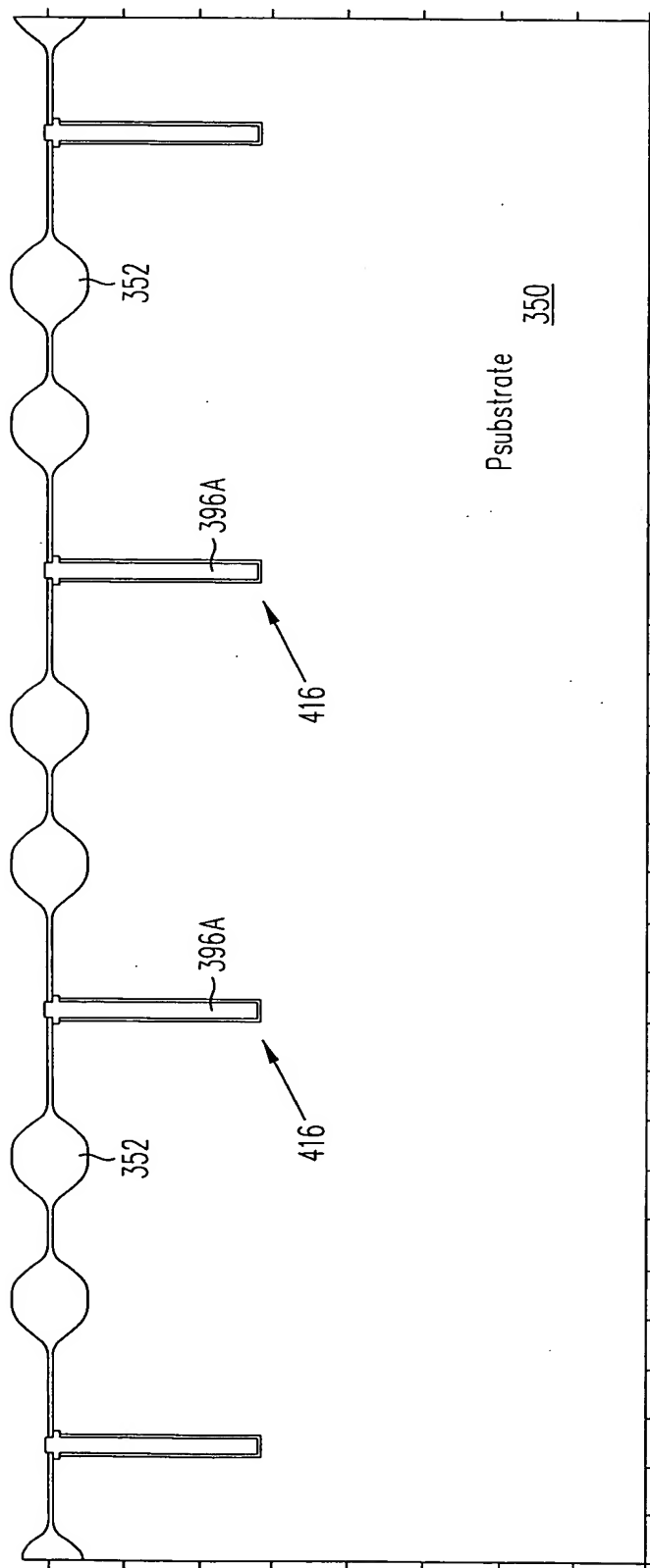
30V Lateral Trench DMOS ~308



Interlayer Dielectric

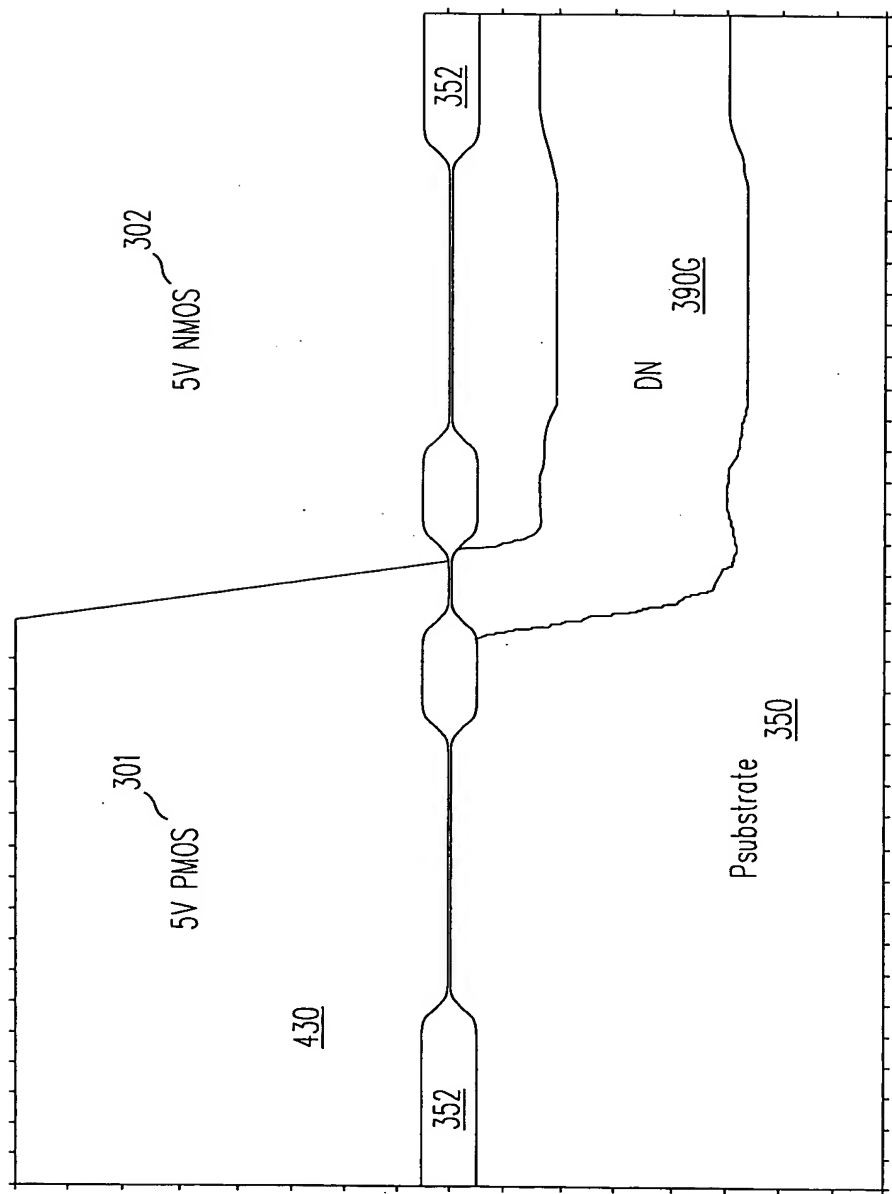
FIG. 33D

30V Lateral Trench DMOS ~ 308



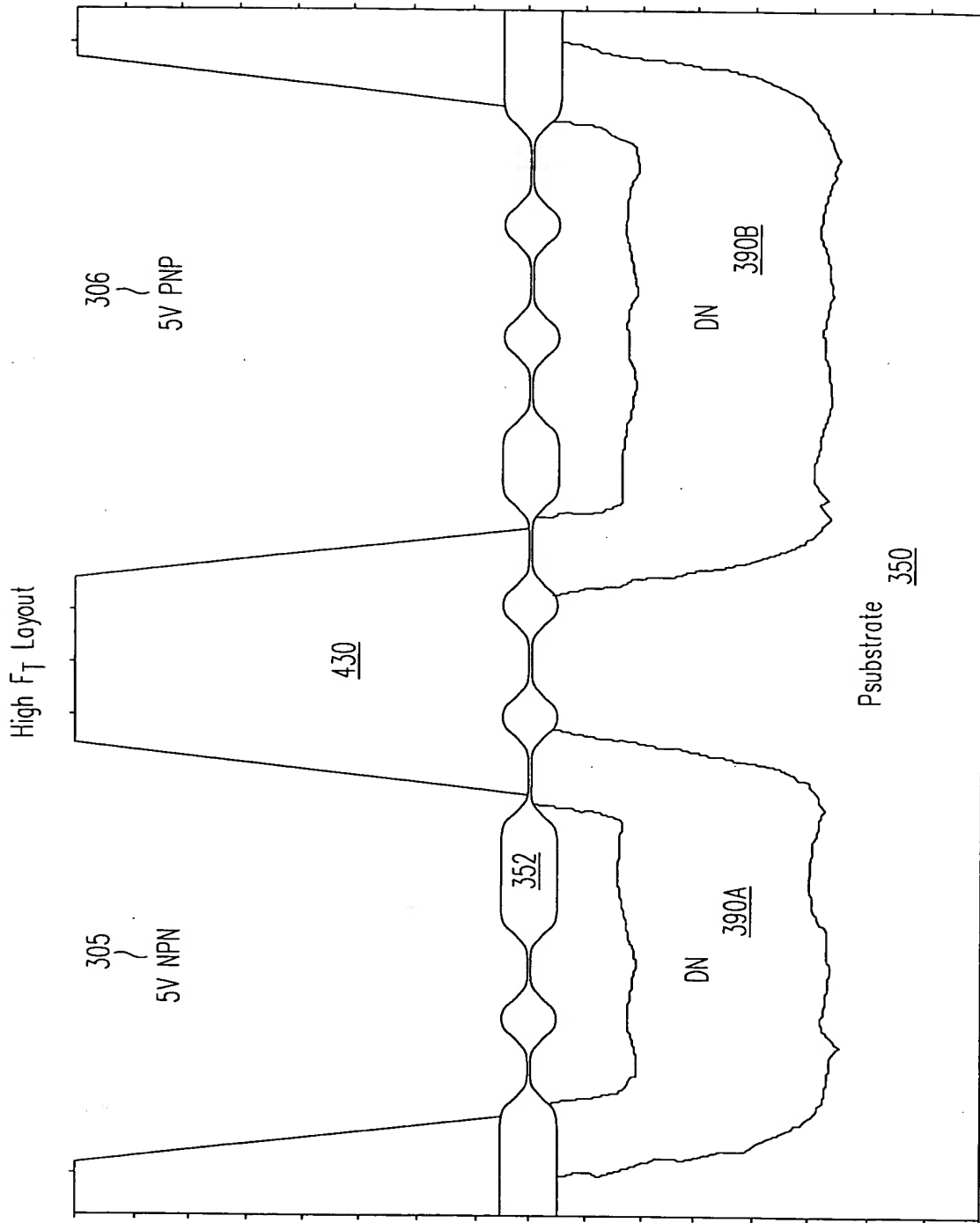
Etchback-Interlayer Dielectric and Second Poly

FIG. 34D



Deep N Mask and Implant

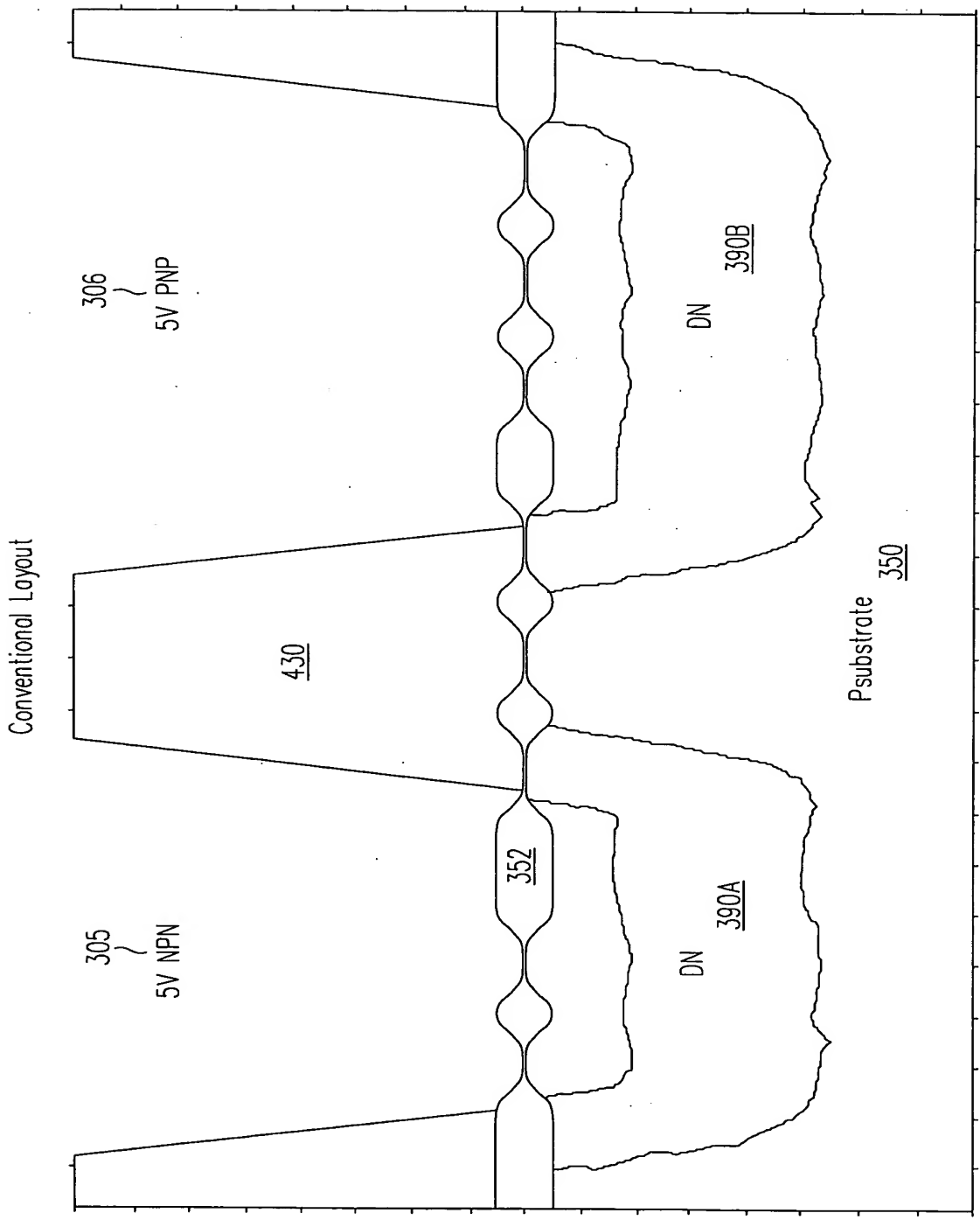
FIG. 35A



Deep N Mask and Implant

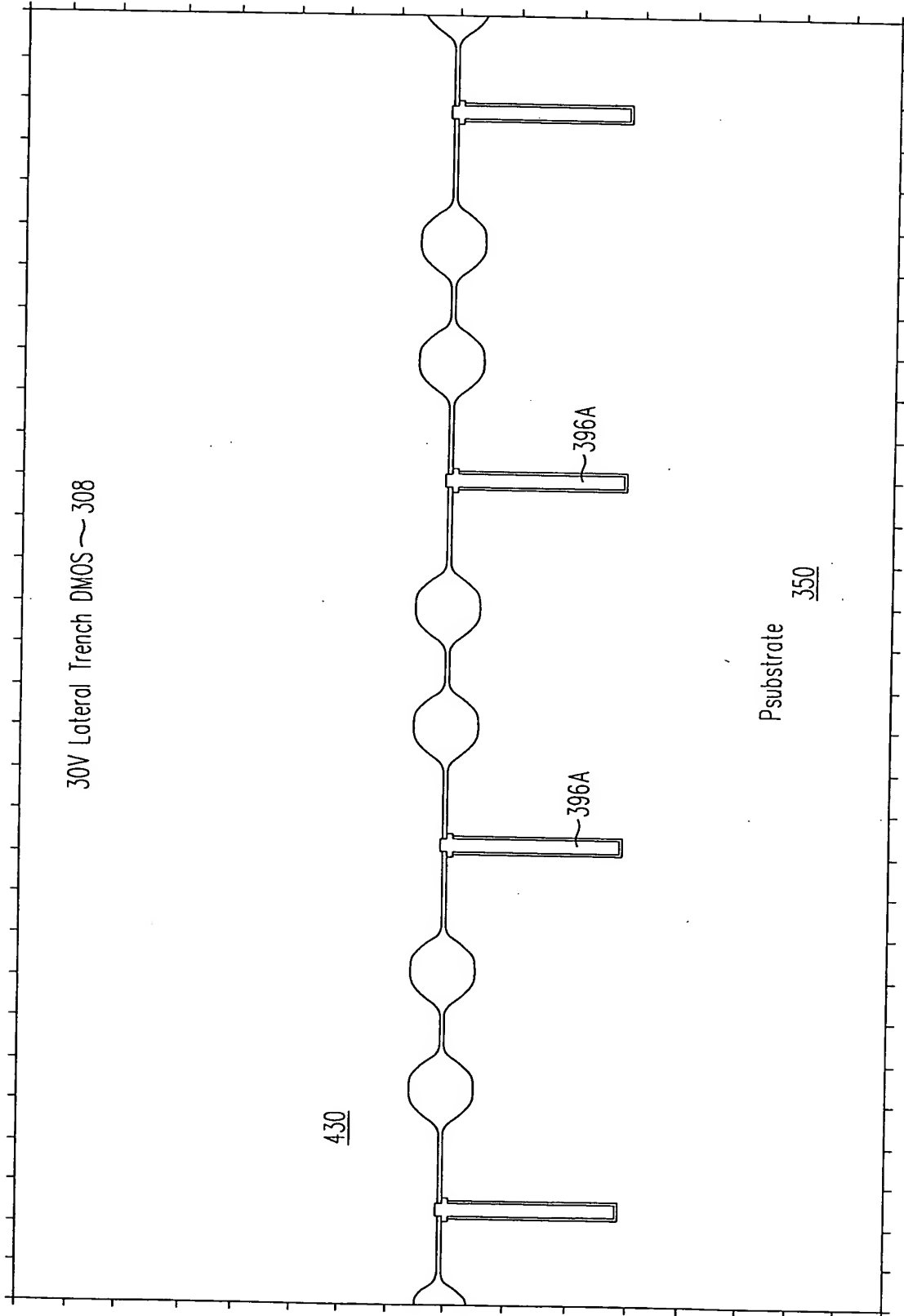
**FIG. 35B**





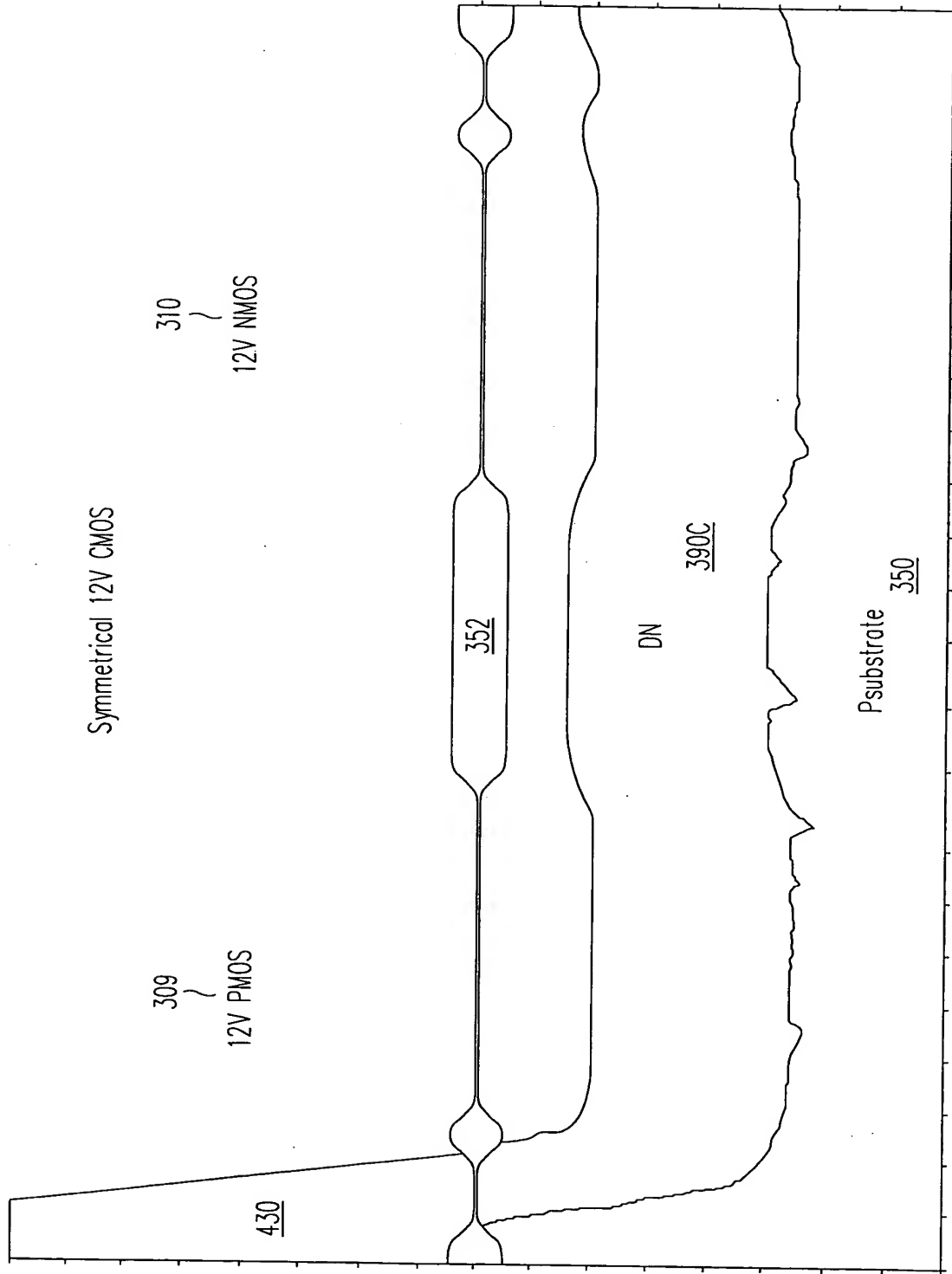
Deep N Mask and Implant

FIG. 35C



Deep N Mask and Implant

FIG. 35D



Deep N Mask and Implant

FIG. 35E

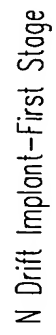
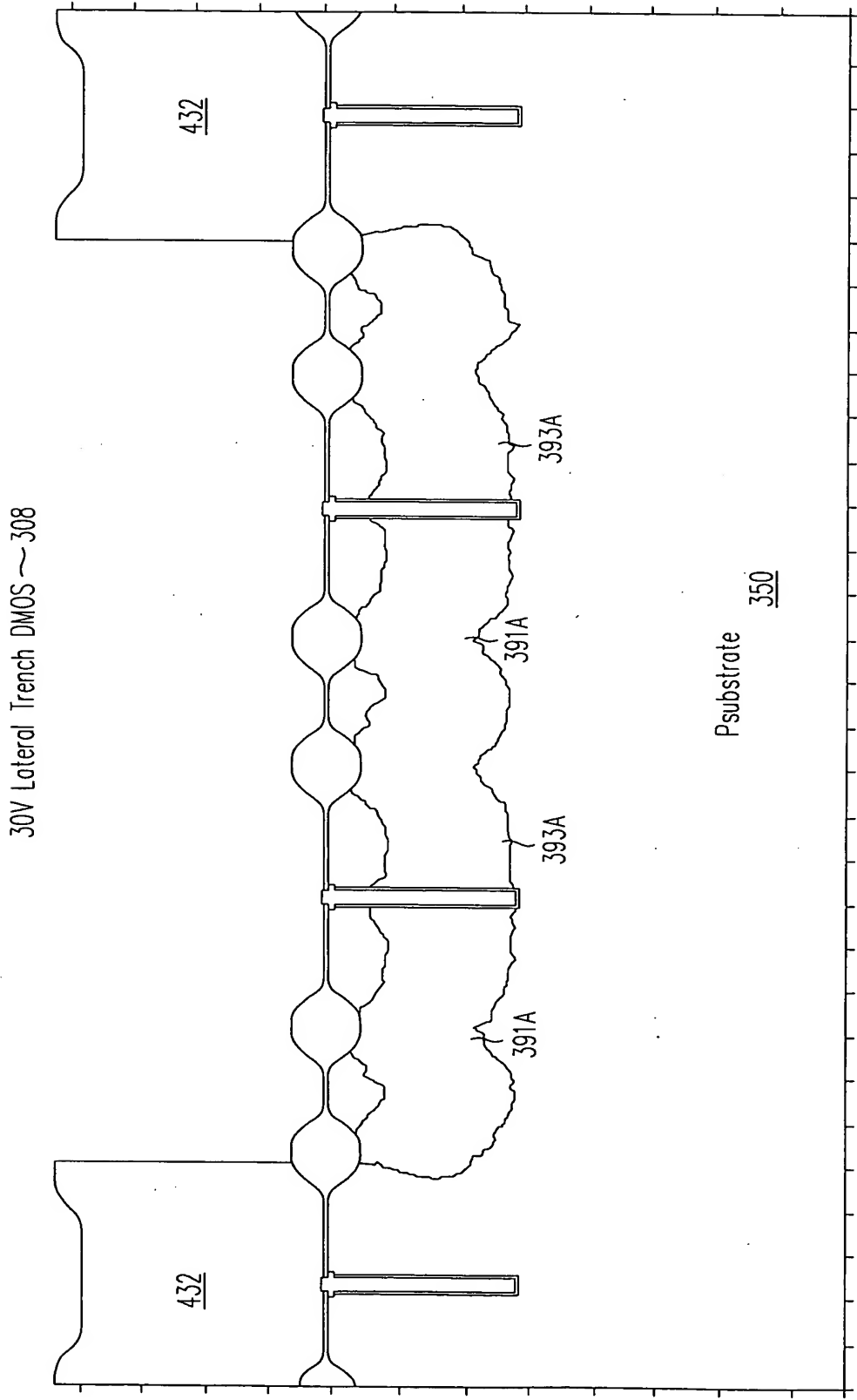
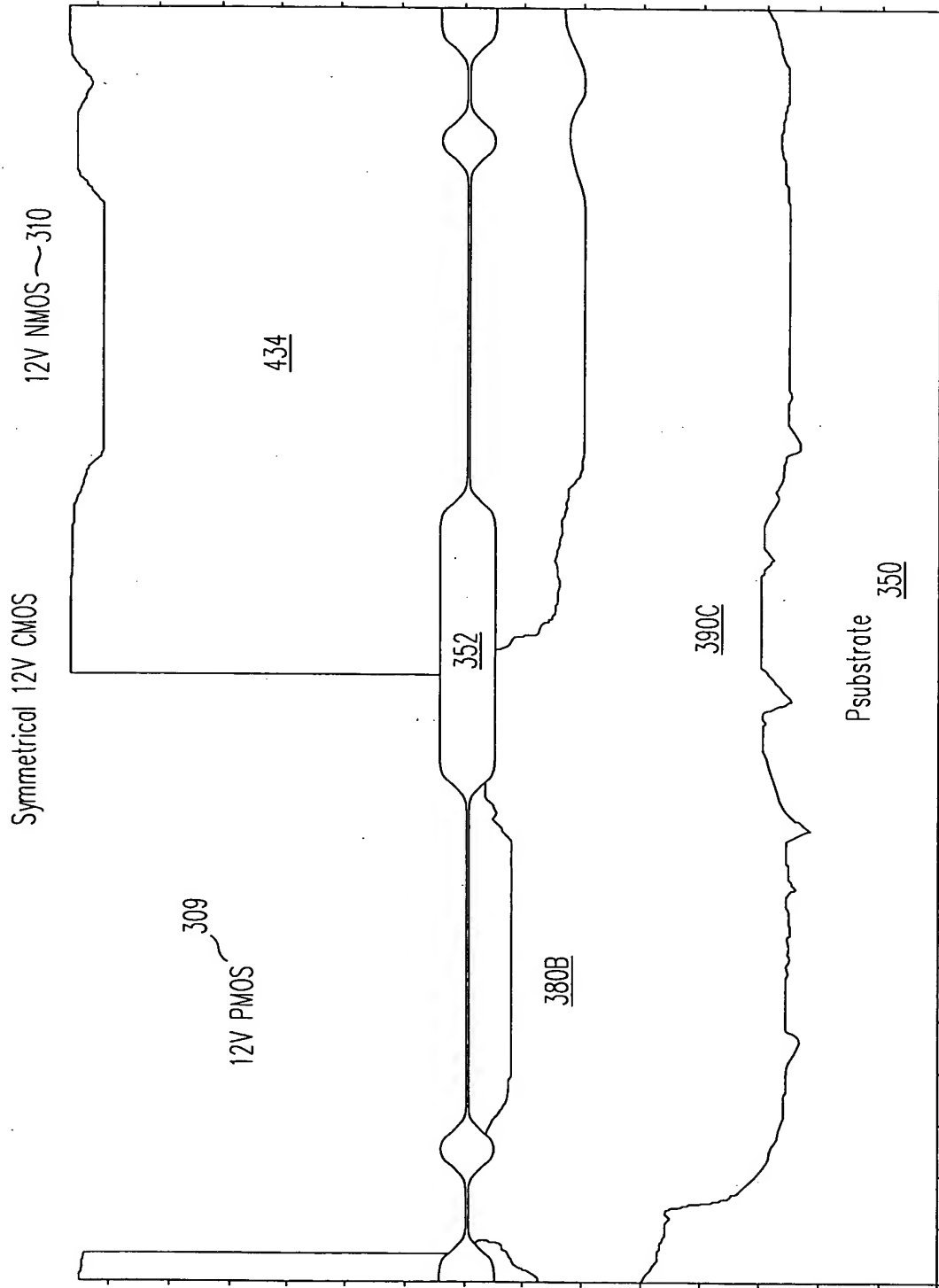


FIG. 36D



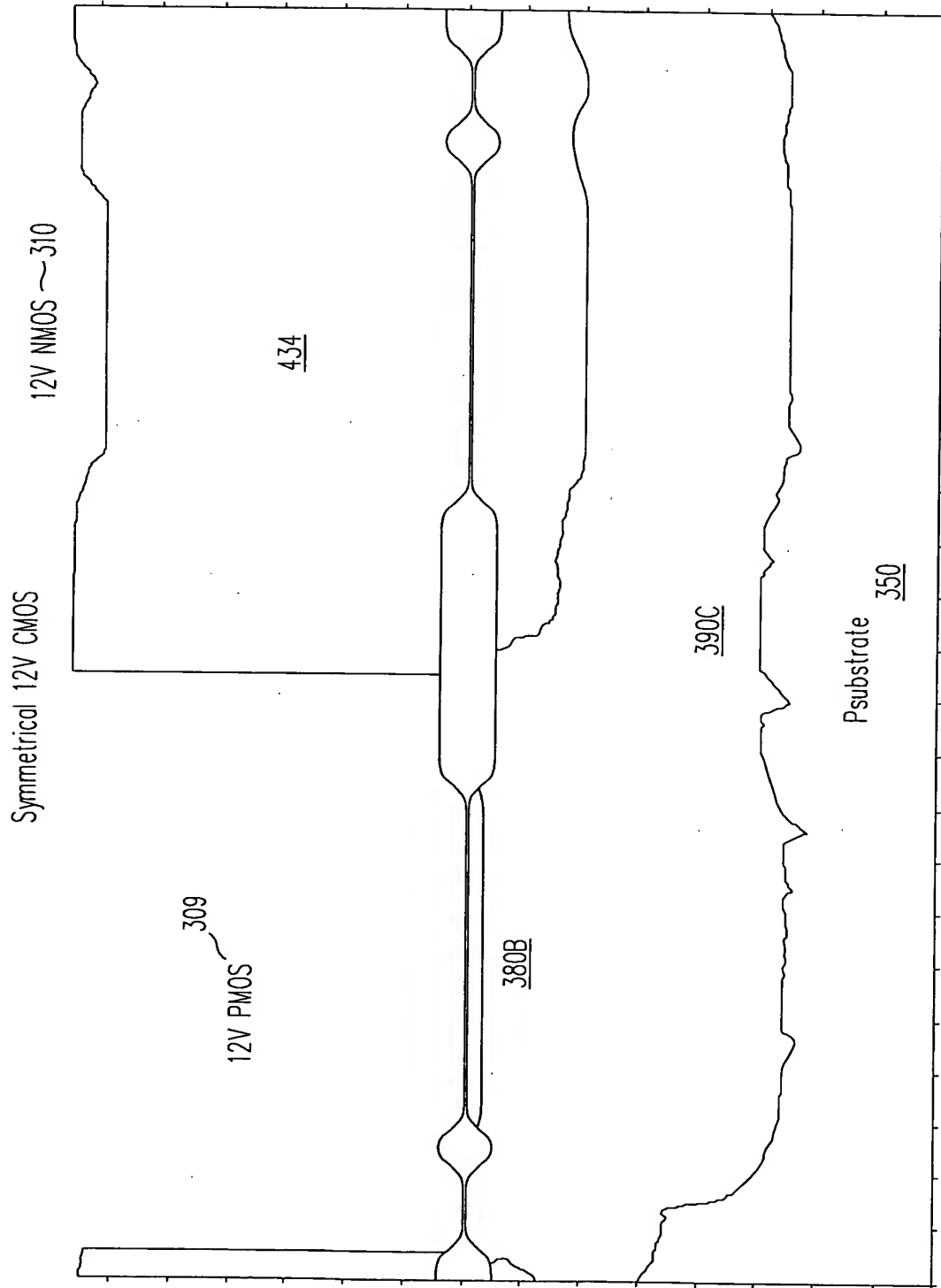
N Drift Implant-Second Stage

FIG. 37D



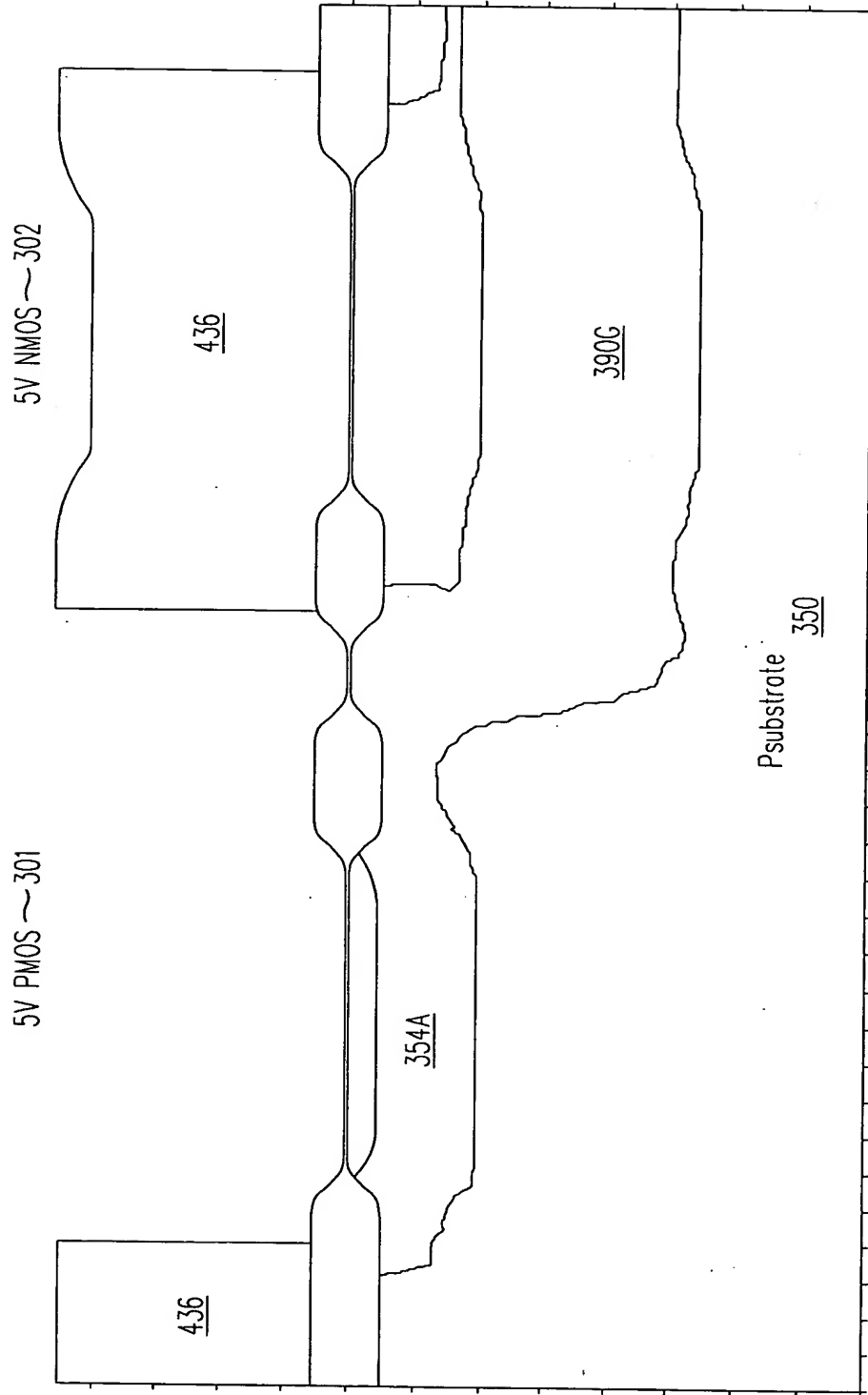
12V N Well Implant-First Stage

*FIG. 38E*



12V N Well Implant-Second Stage

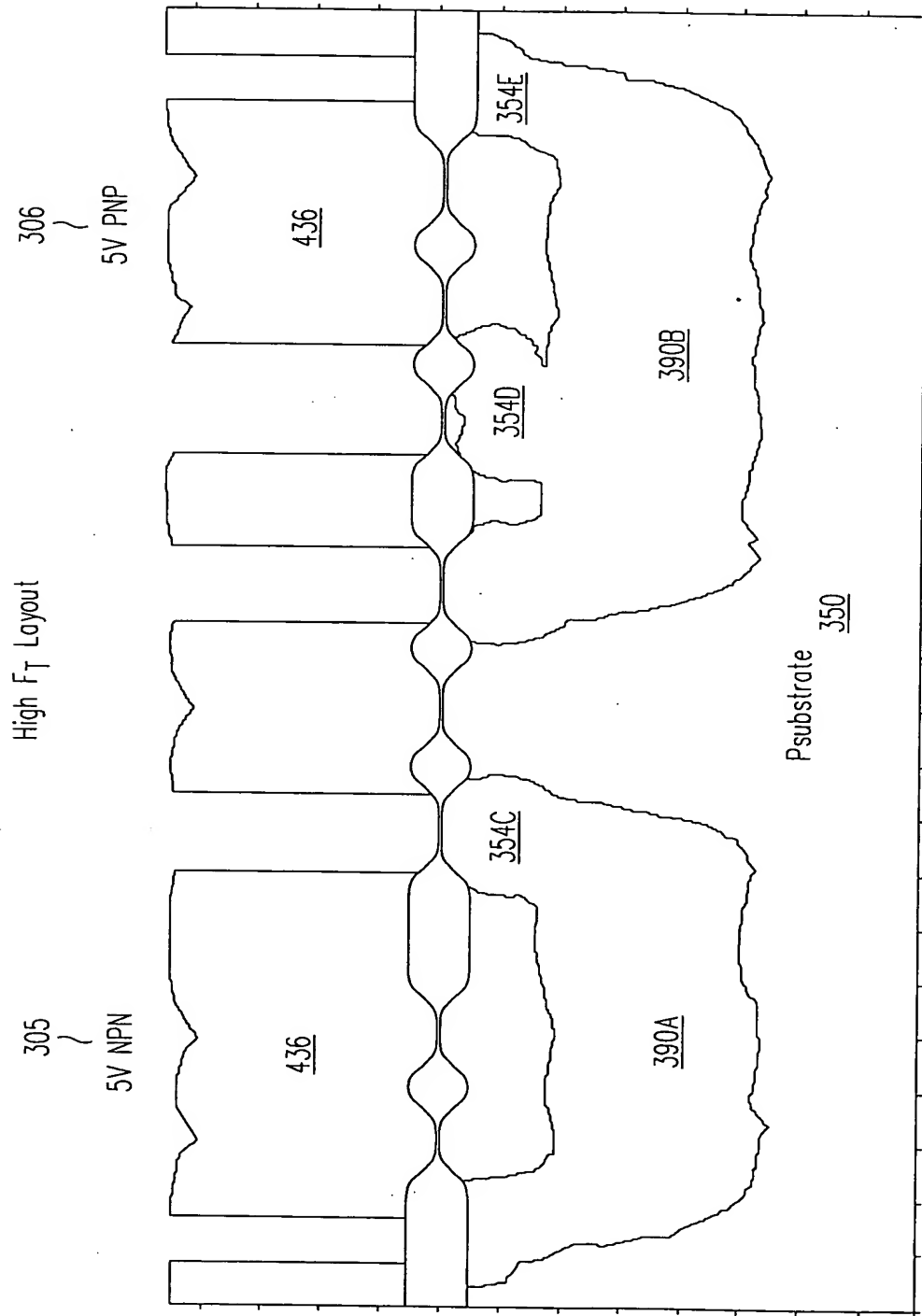
*FIG. 39E*



5V N Well Implant-First Stage

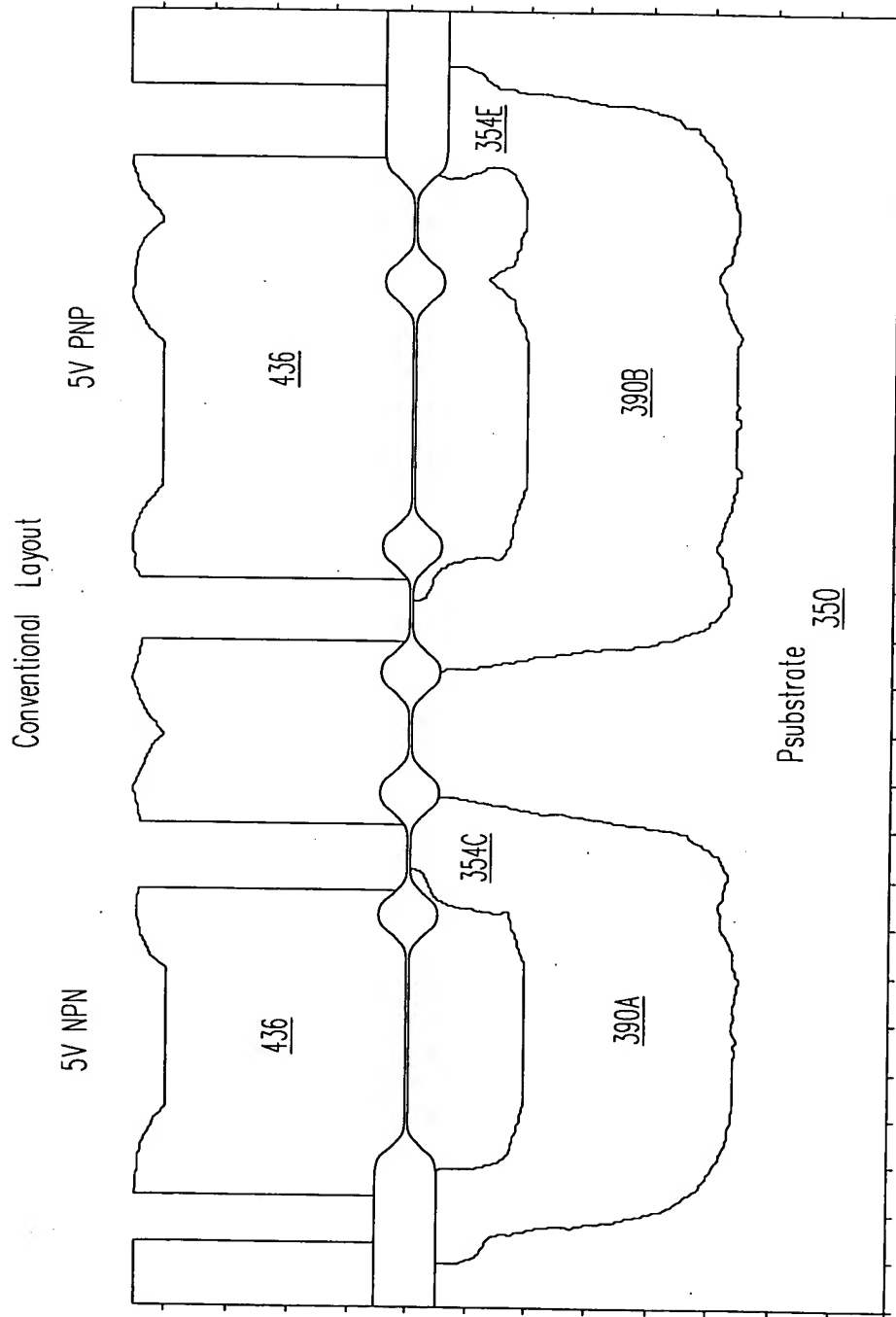
*FIG. 40A*





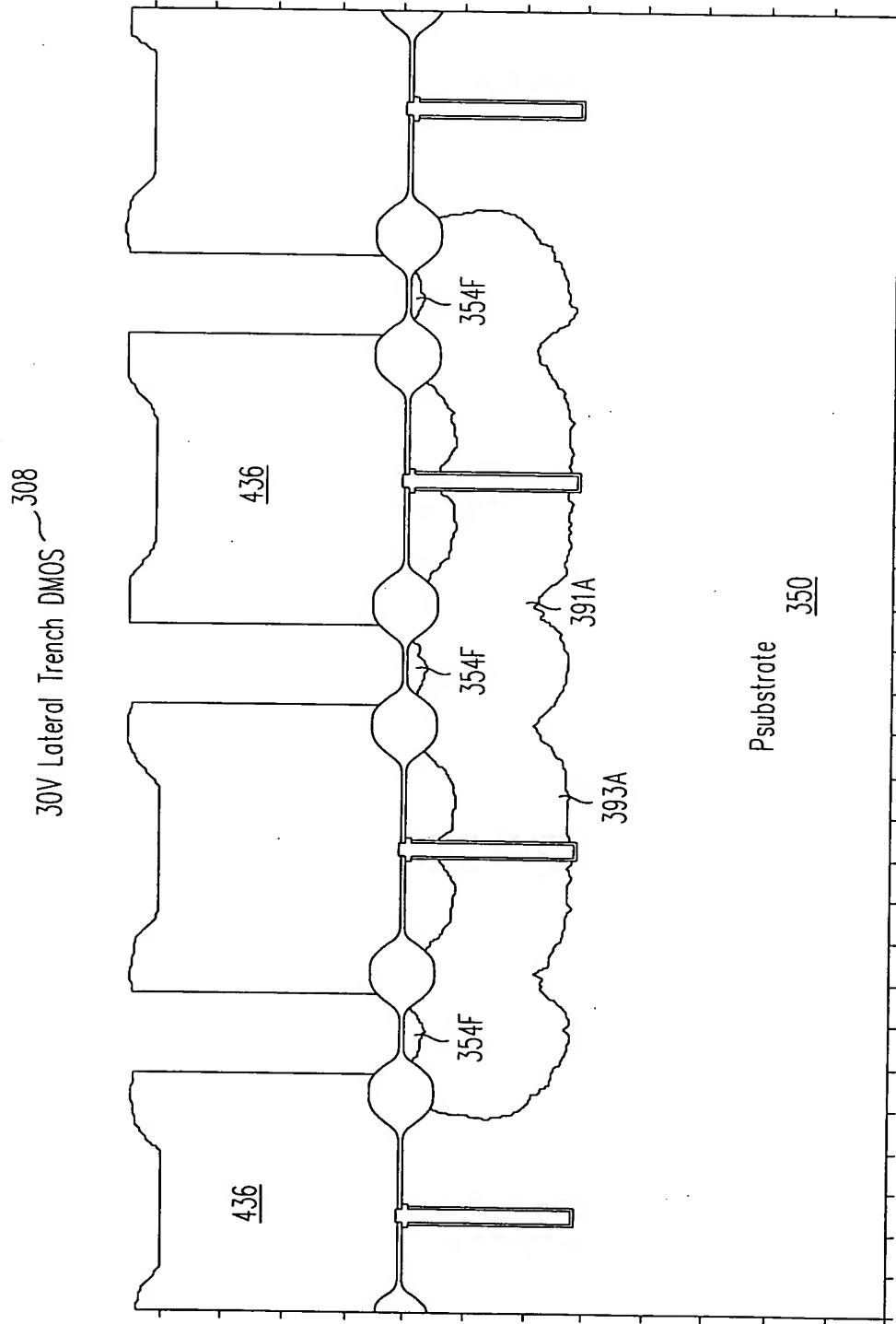
5V N Well Implant-First Stage

FIG. 40B



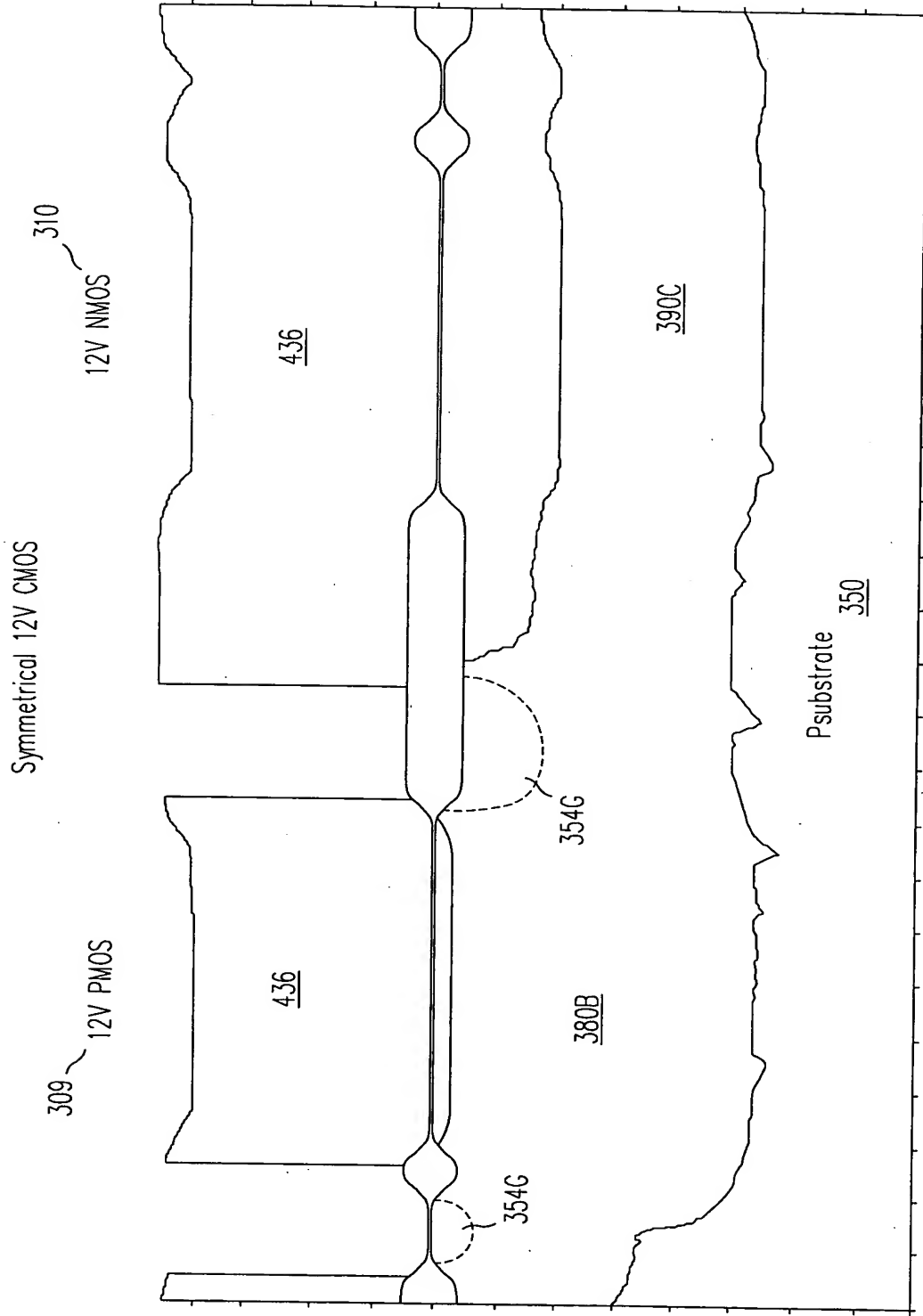
5V N Well Implant-First Stage

*FIG. 40C*



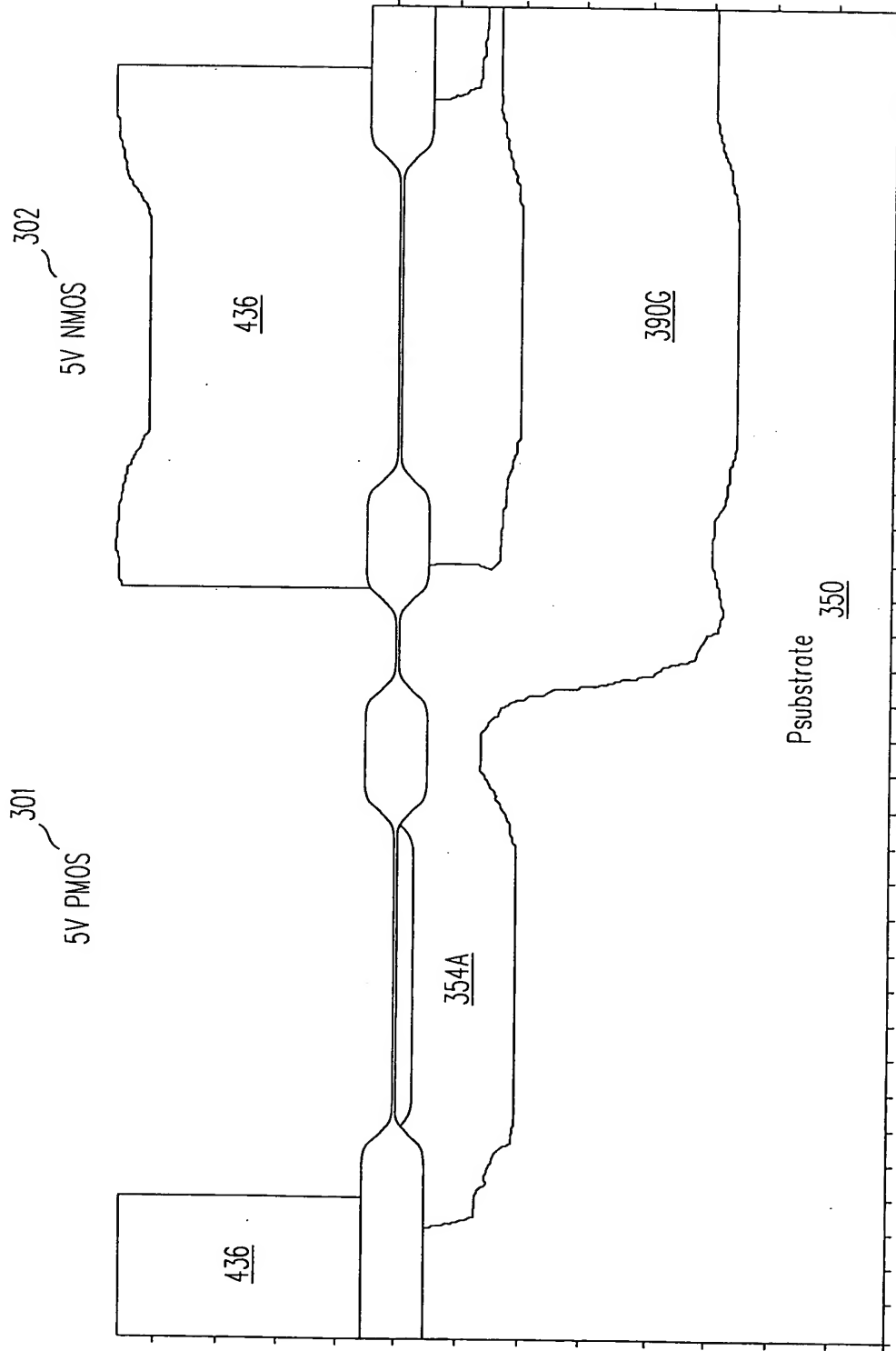
5V N Well Implant-First Stage

FIG. 40D



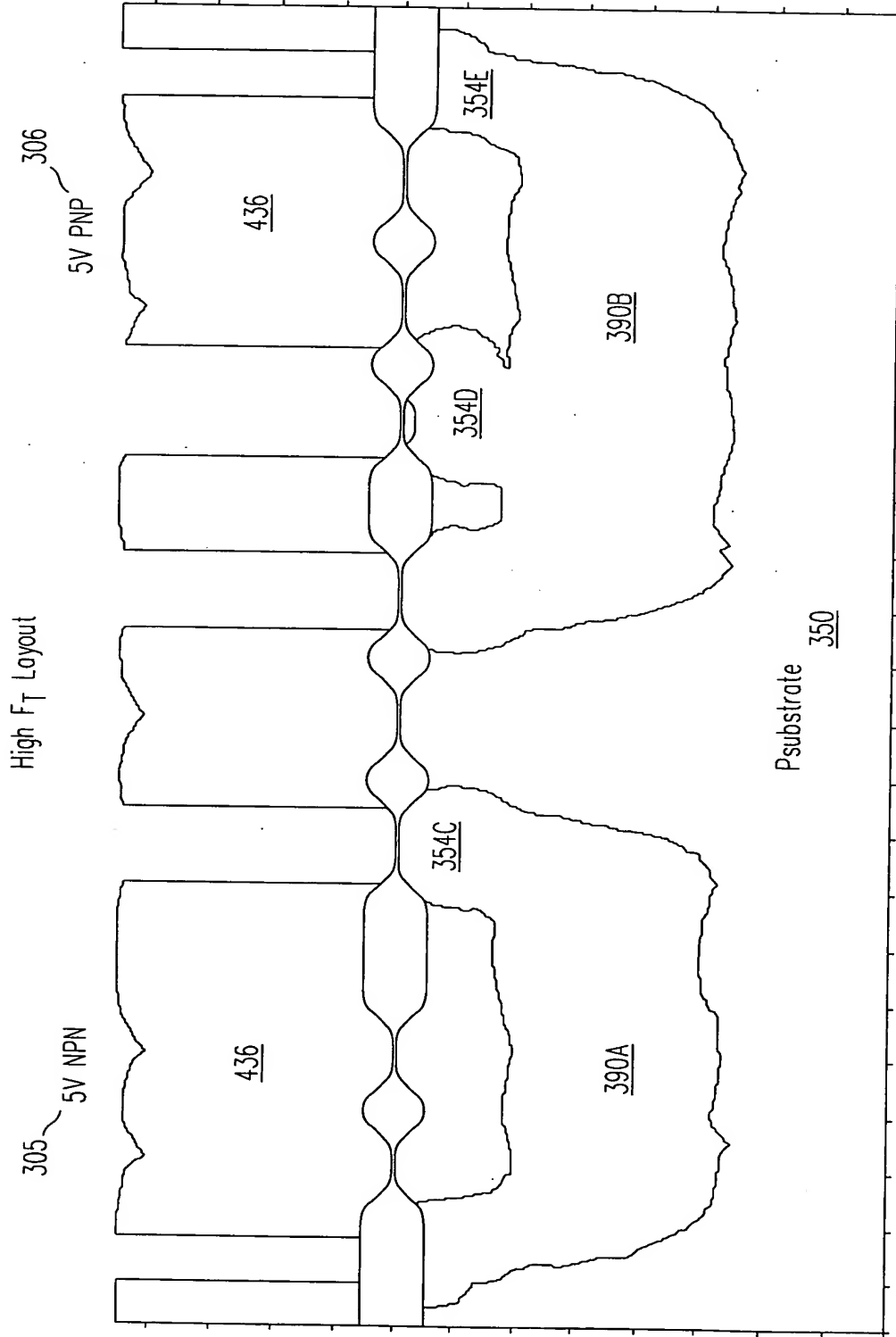
5V N Well Implant-First Stage

**FIG. 40E**



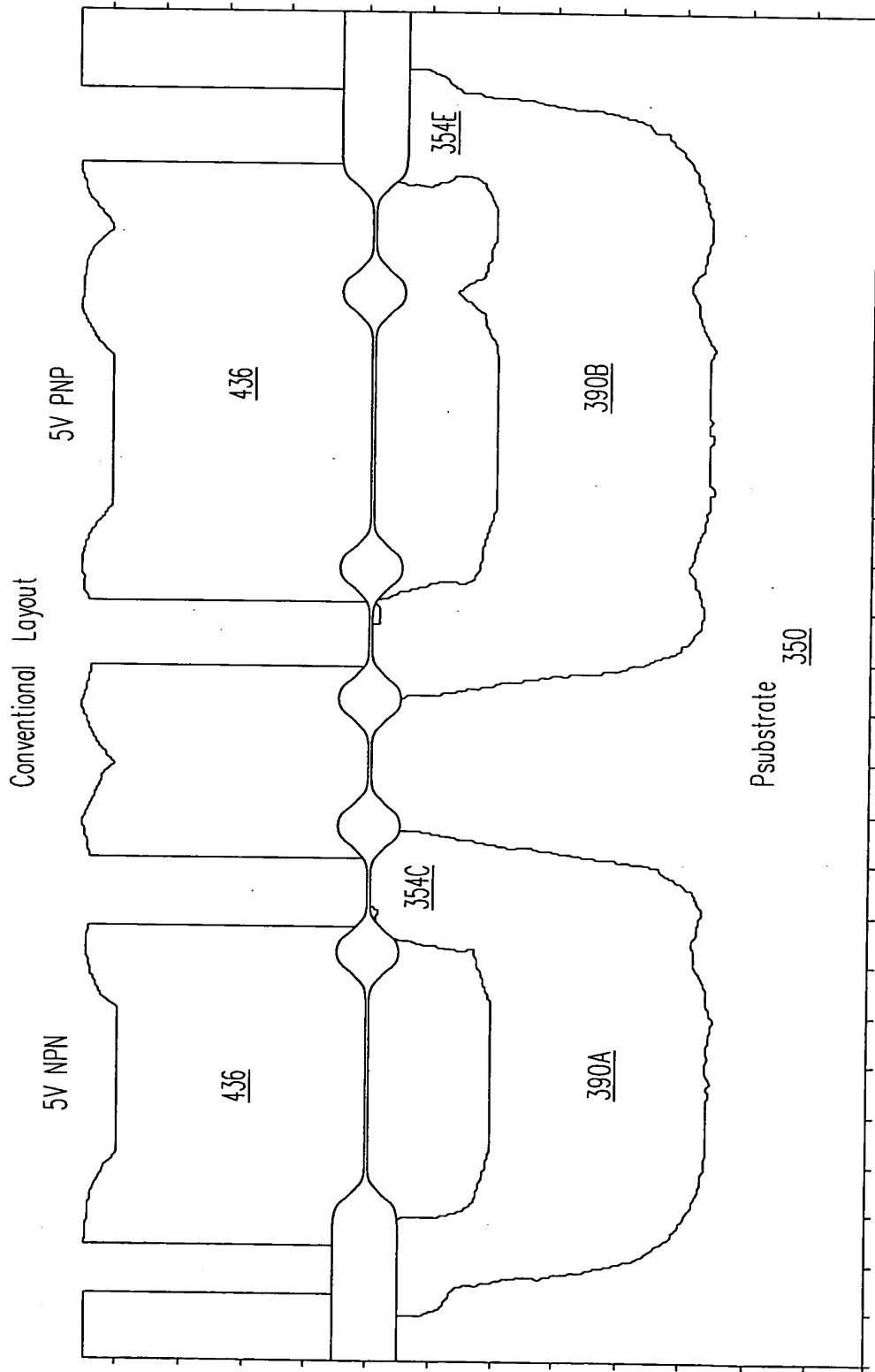
5V N Well Implant—Second Stage

*FIG. 41A*



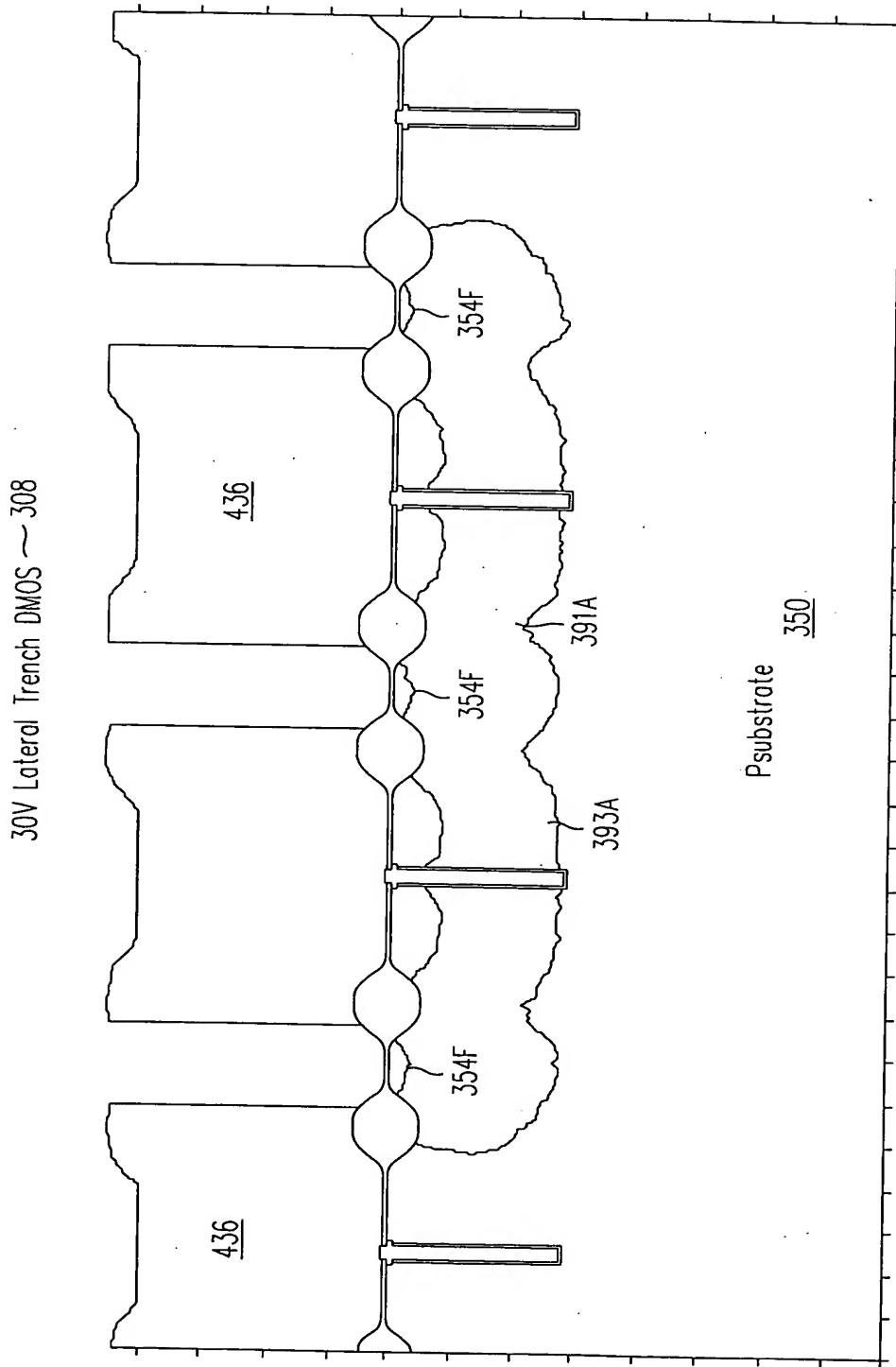
5V N Well Implant-Second Stage

FIG. 41B



5V N Well Implant-Second Stage

*FIG. 41C*

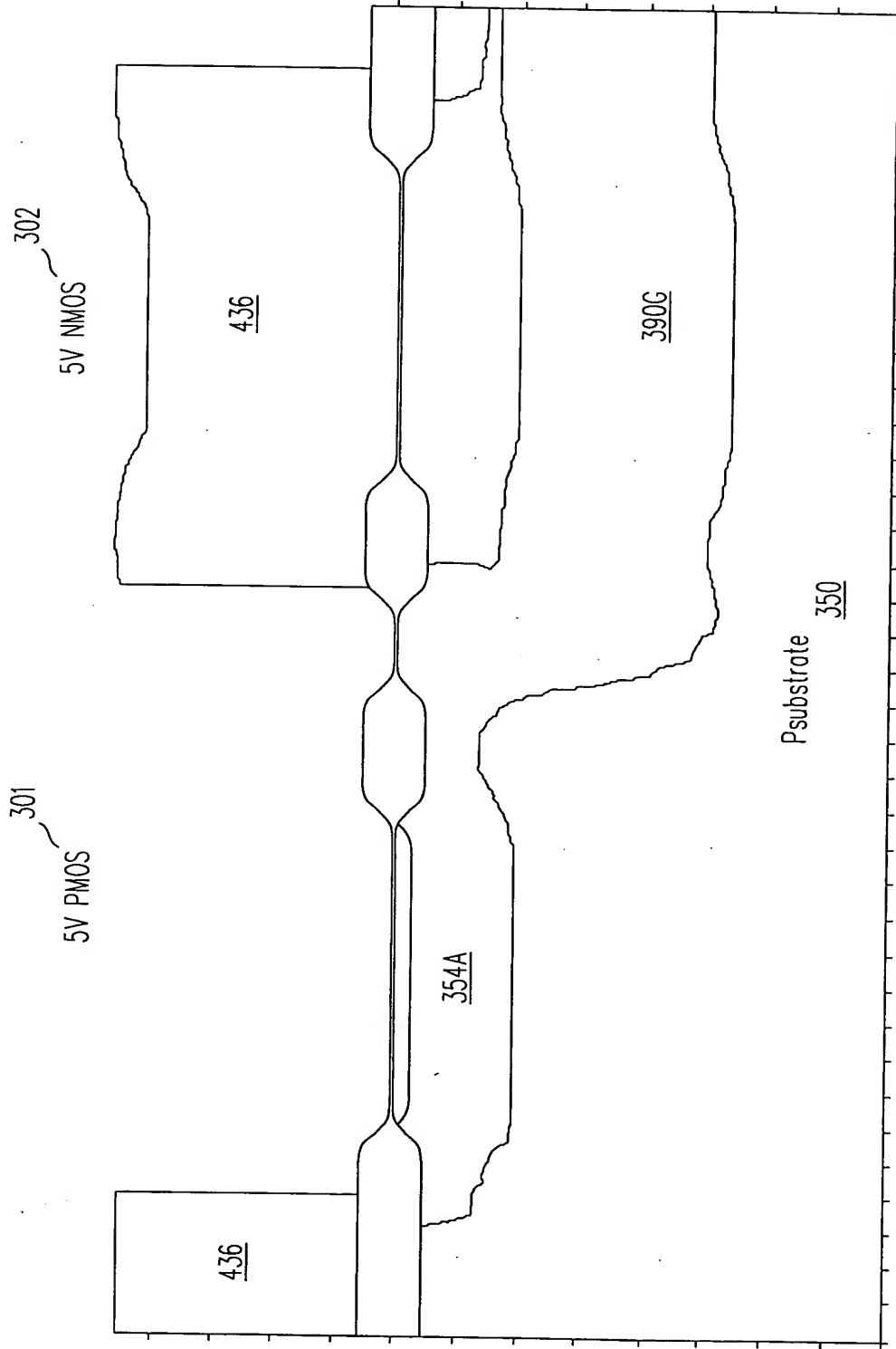


5V N Well Implant—Second Stage

*FIG. 41D*

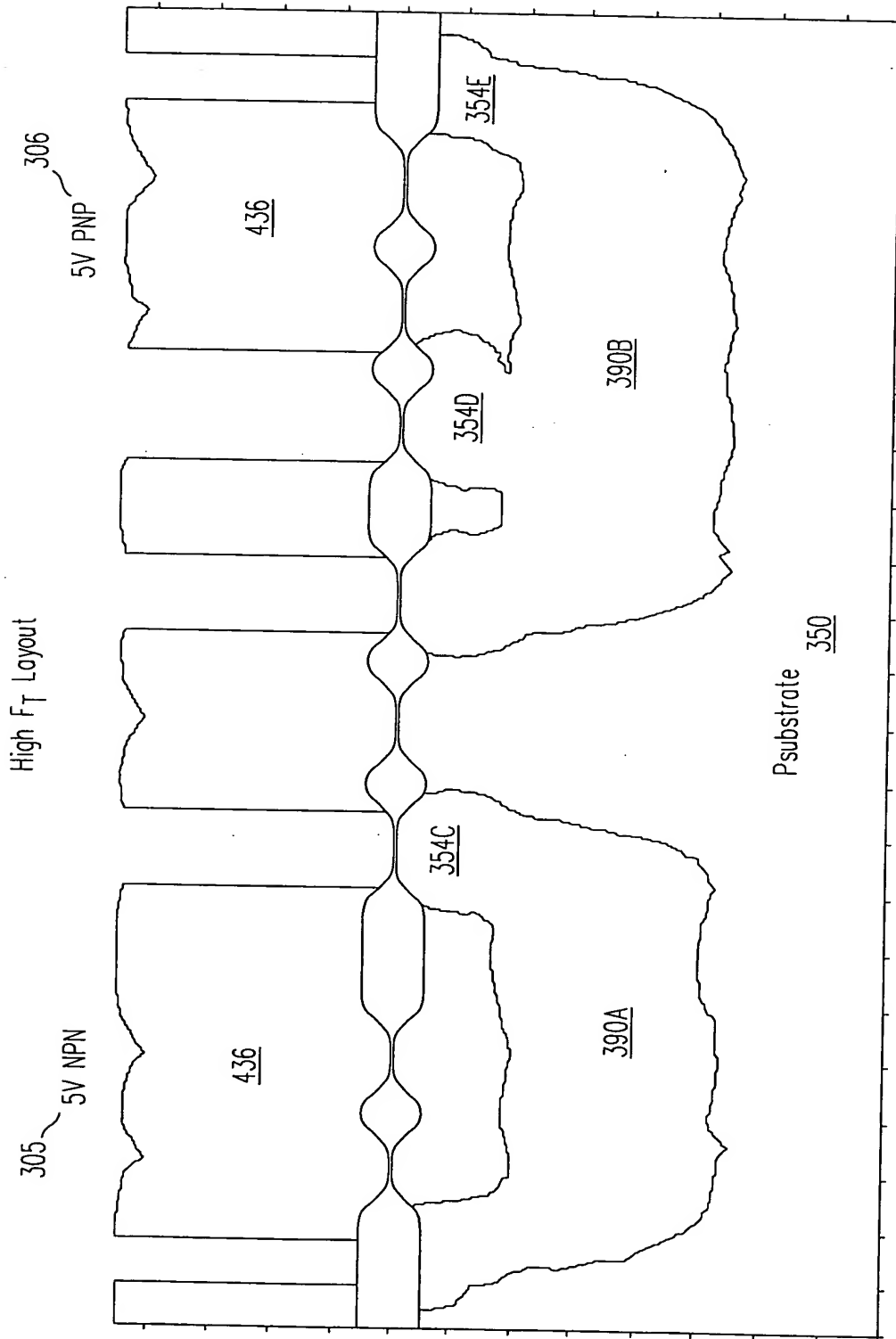






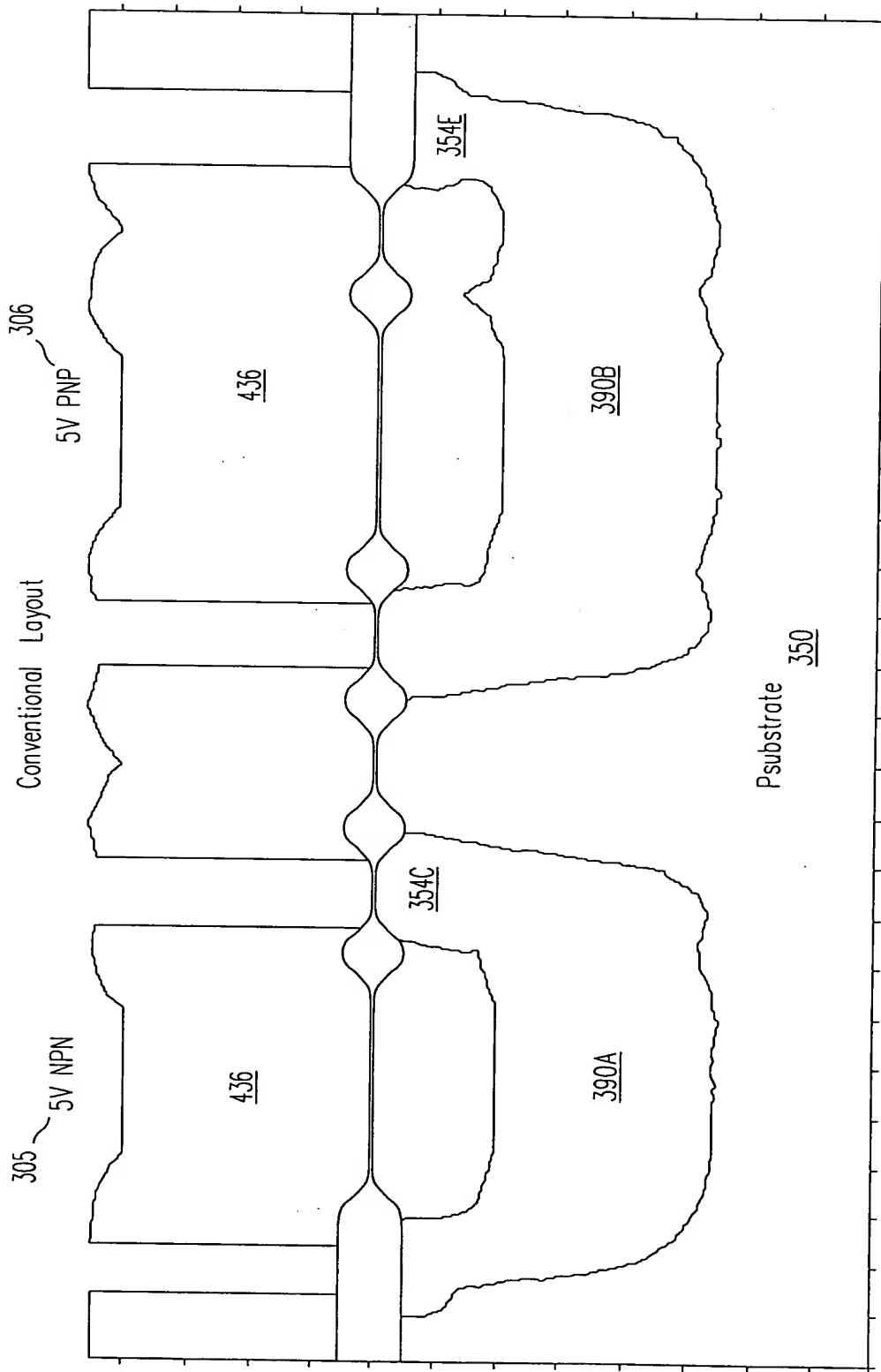
5V N Well Implant-Third Stage

*FIG. 42A*



5V N Well Implant-Third Stage

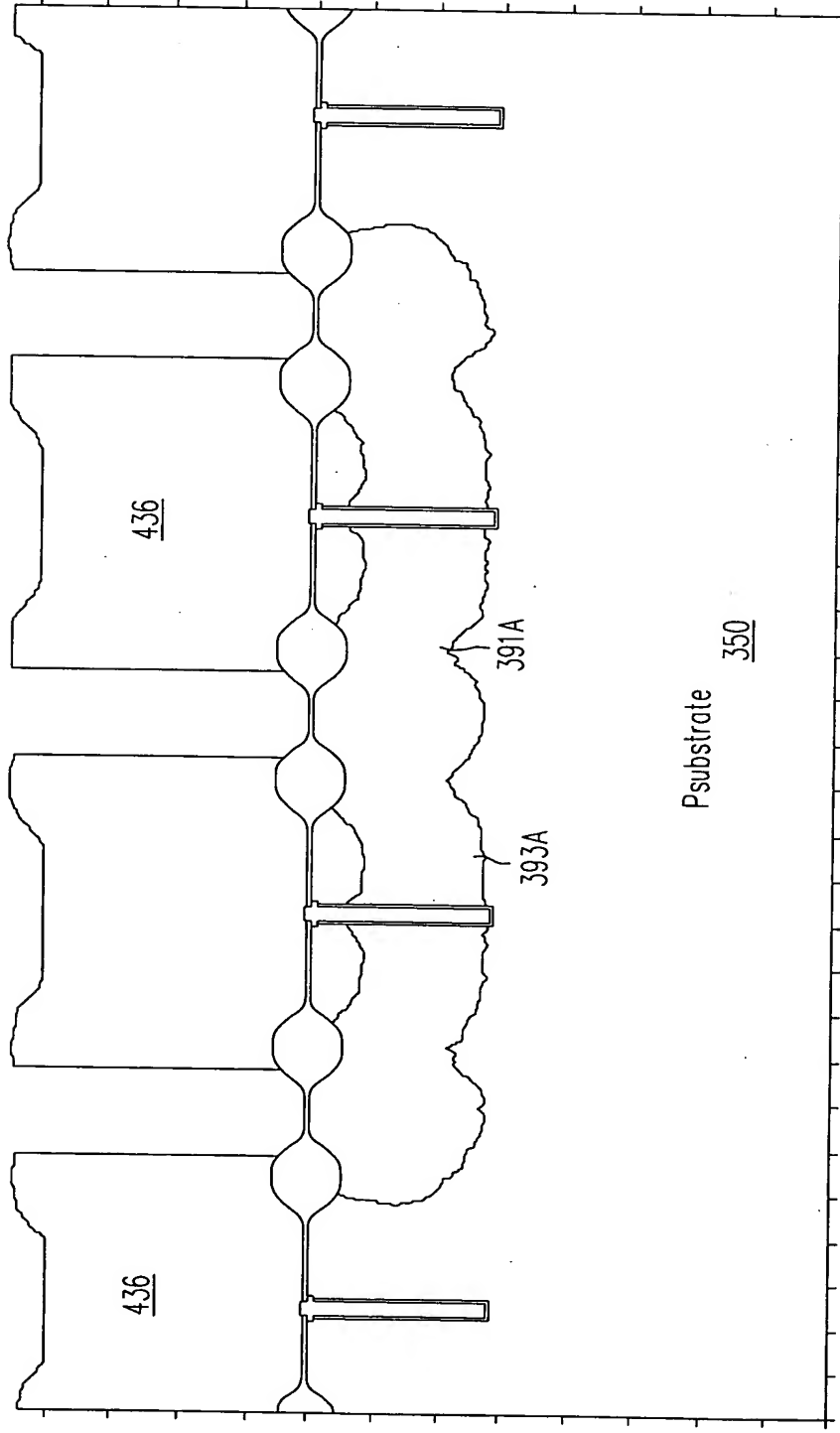
FIG. 42B



5V N Well Implant - Third Stage

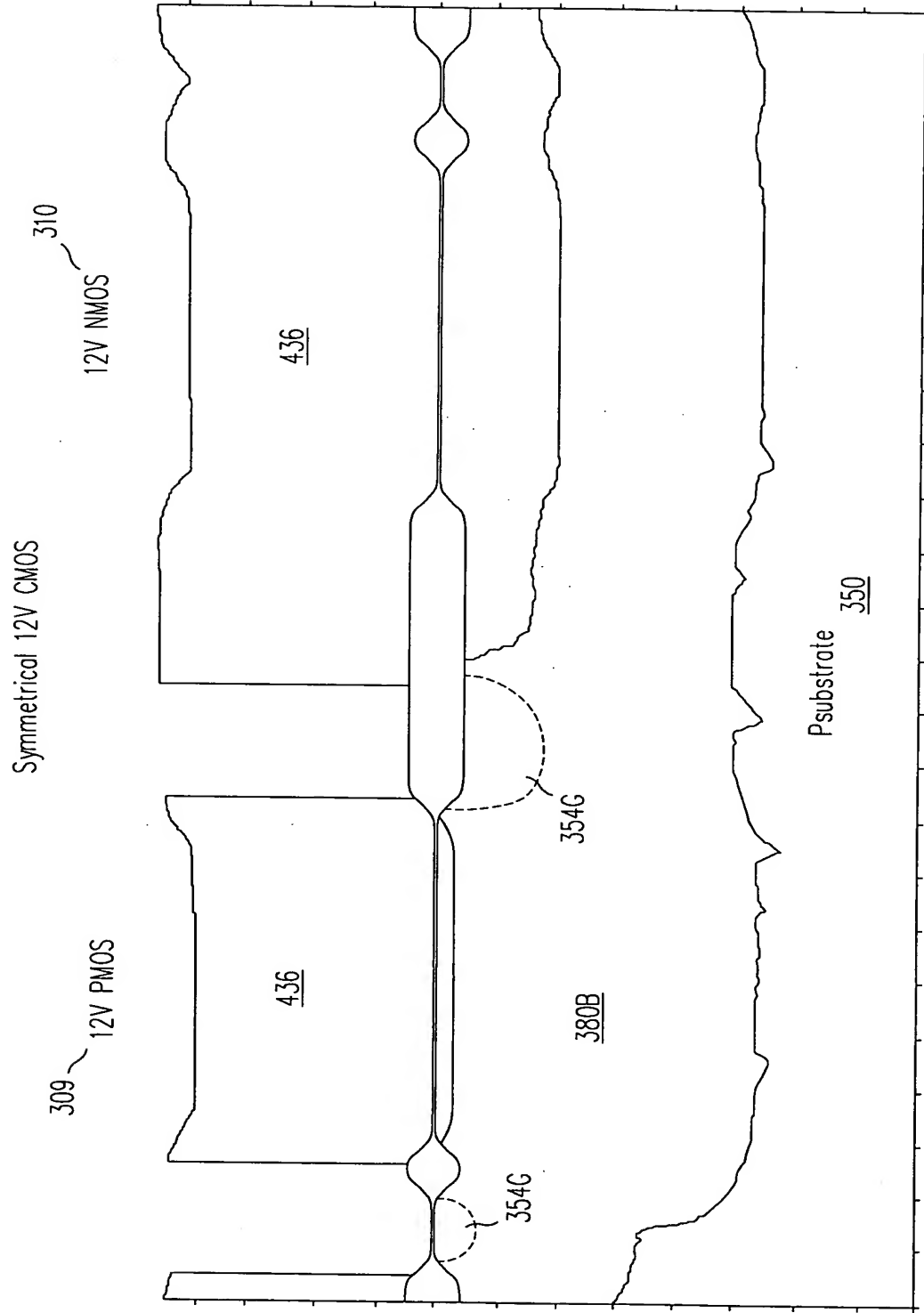
FIG. 42C

30V Lateral Trench DMOS ~ 308



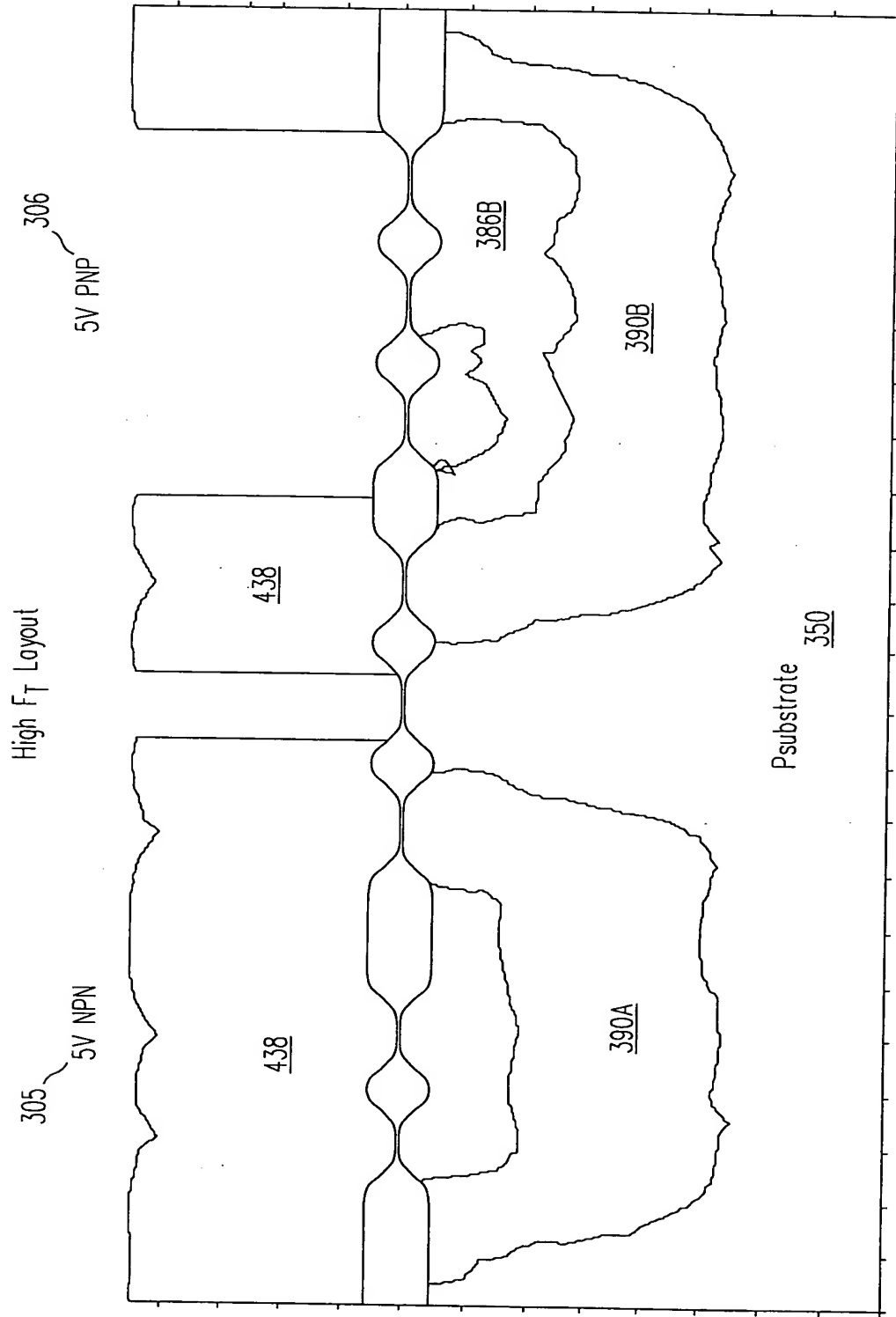
5V N Well Implant—Third Stage

FIG. 42D



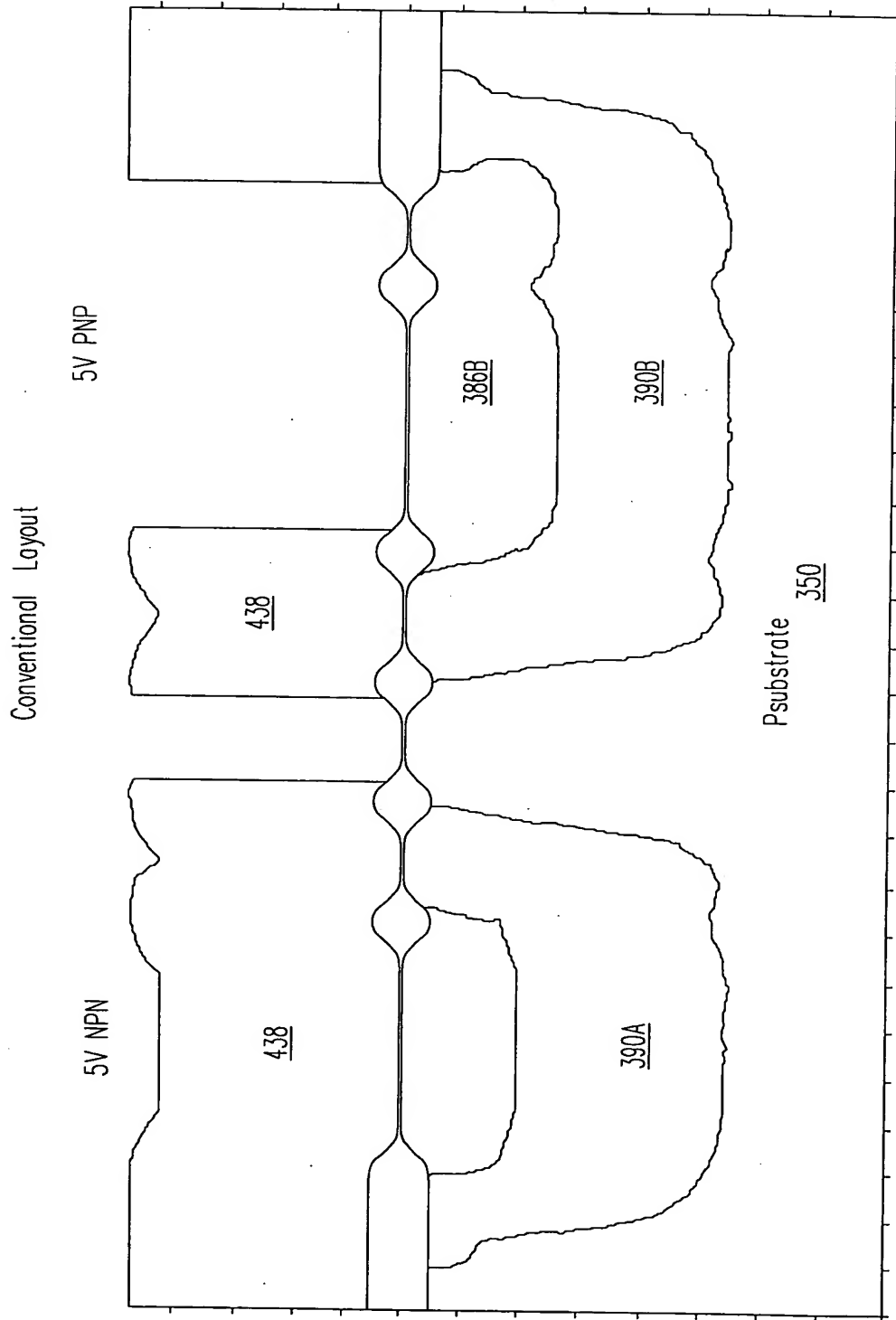
5V N Well Implant - Third Stage

FIG. 42E



12V P Well Implant-First Stage

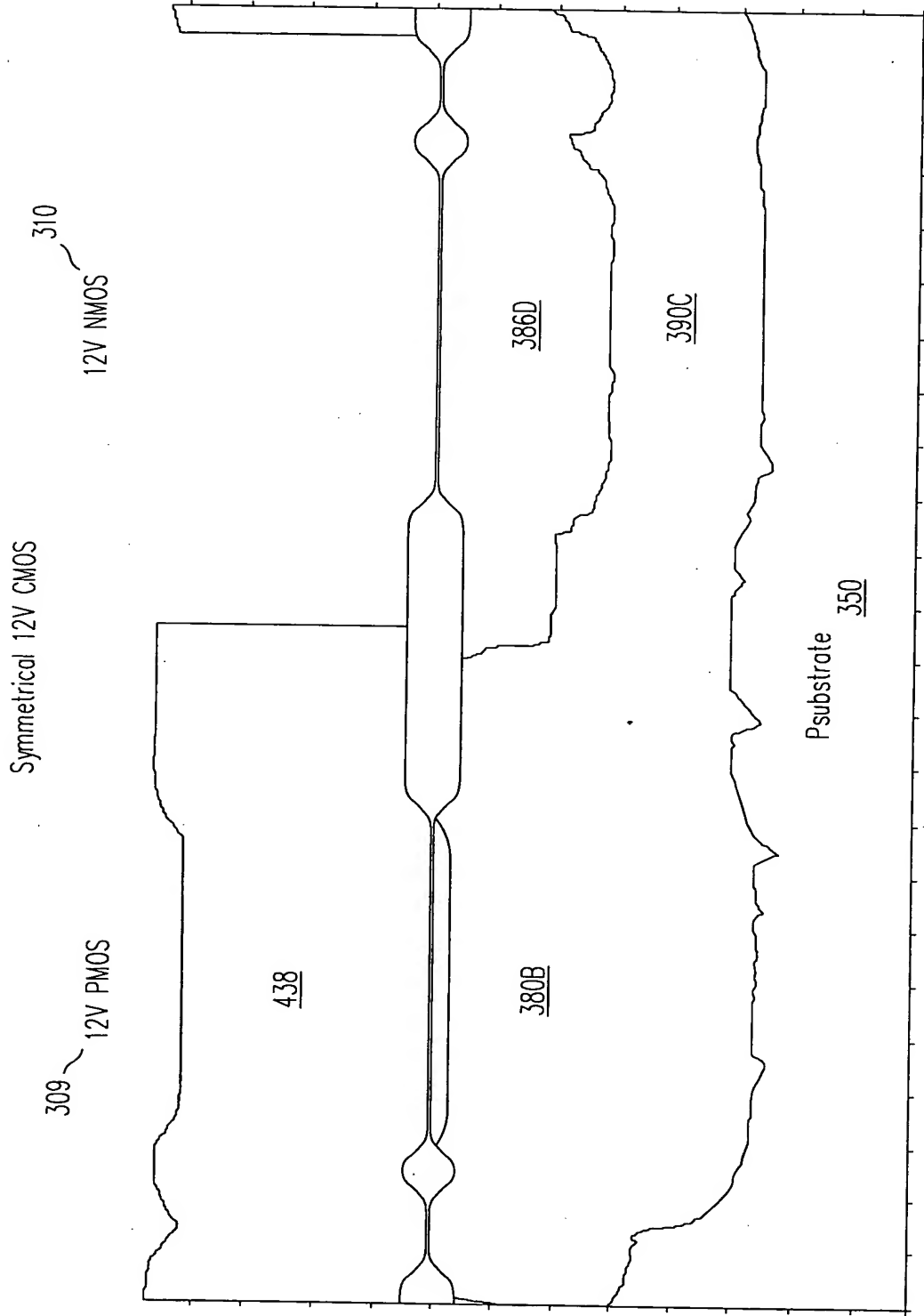
FIG. 43B



12V P Well Implant-First Stage

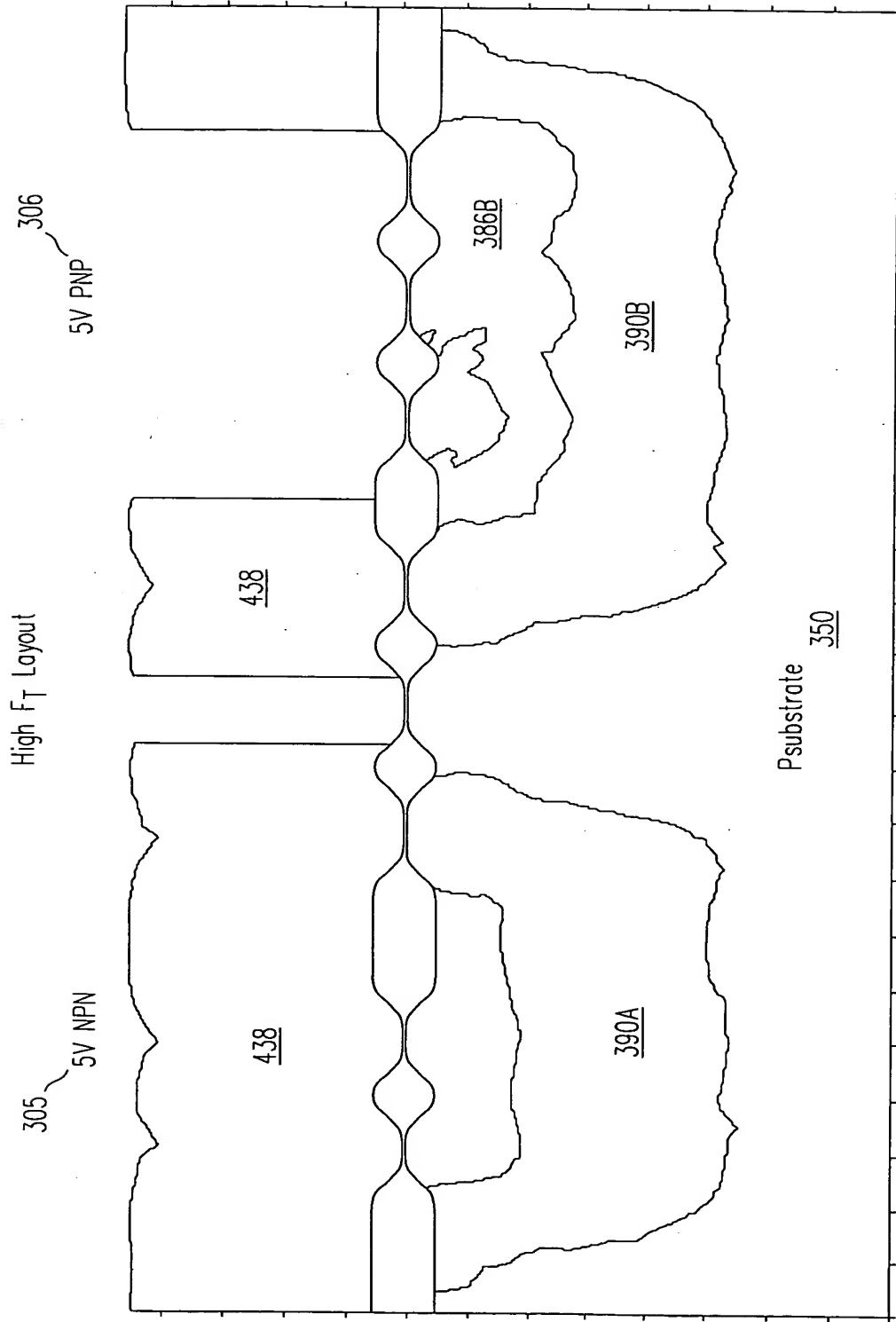
FIG. 43C





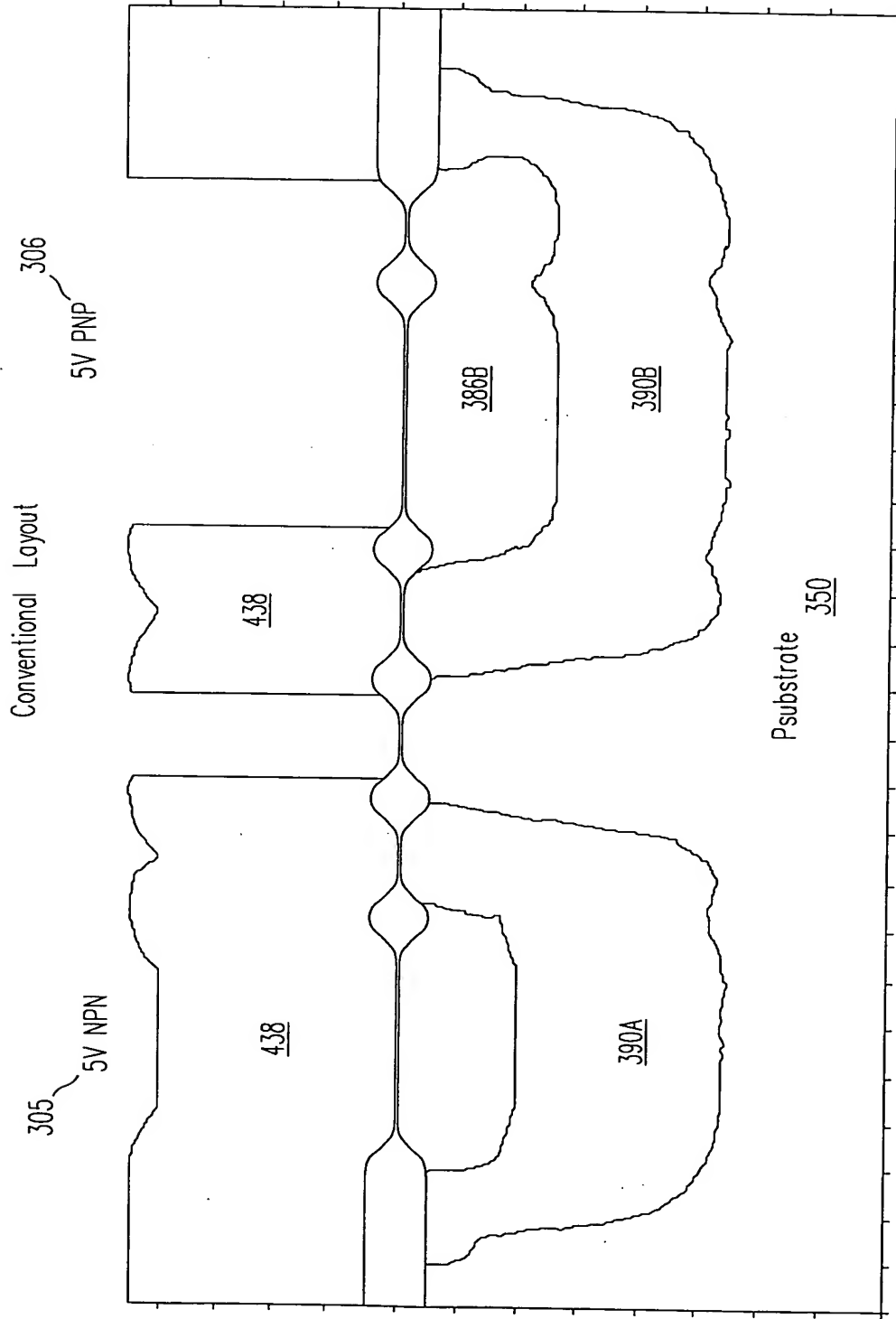
12V P Well Implant-First Stage

*FIG. 43E*



12V P Well Implant-Second Stage

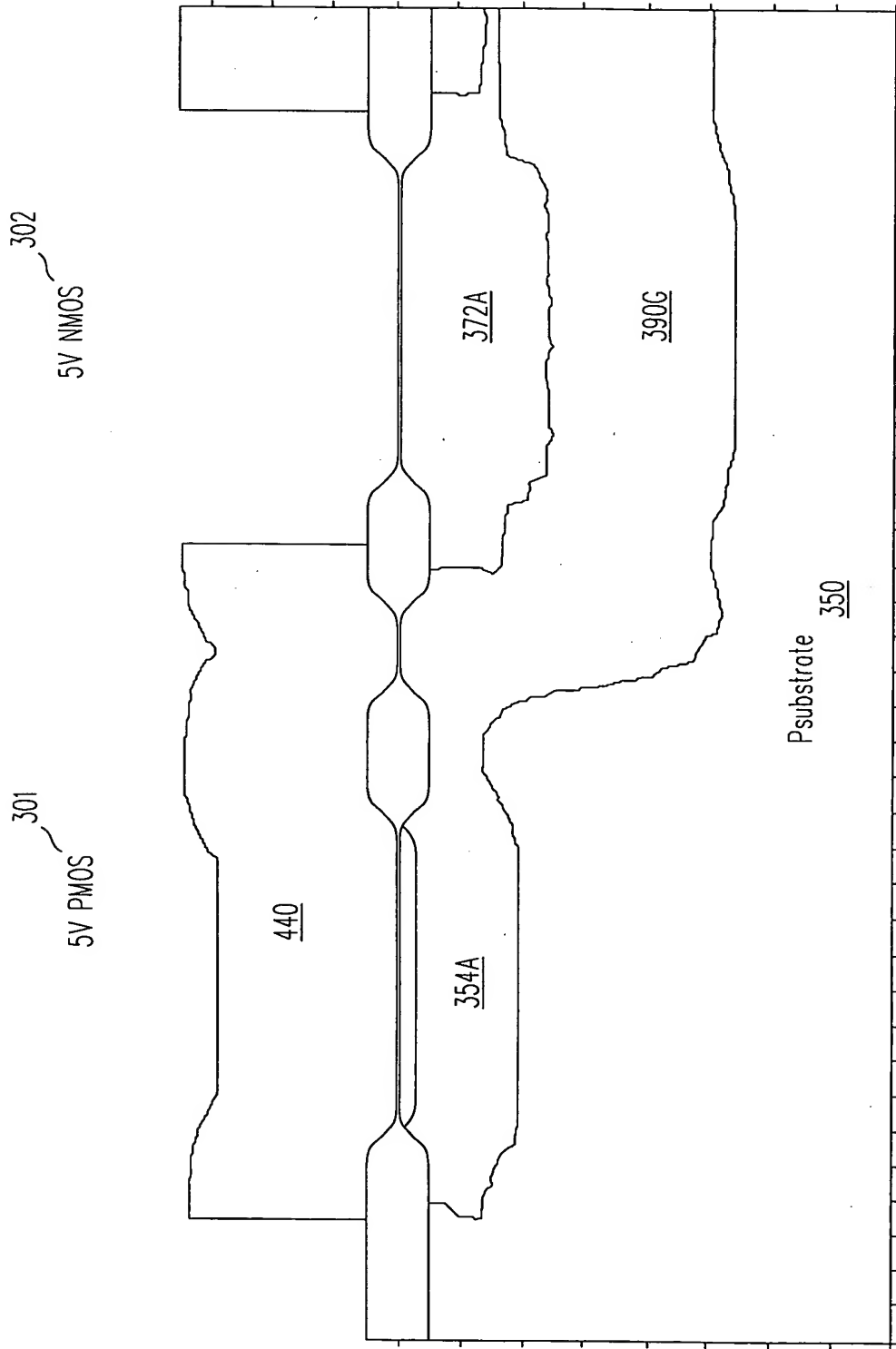
**FIG. 44B**



12V P Well Implant-Second Stage

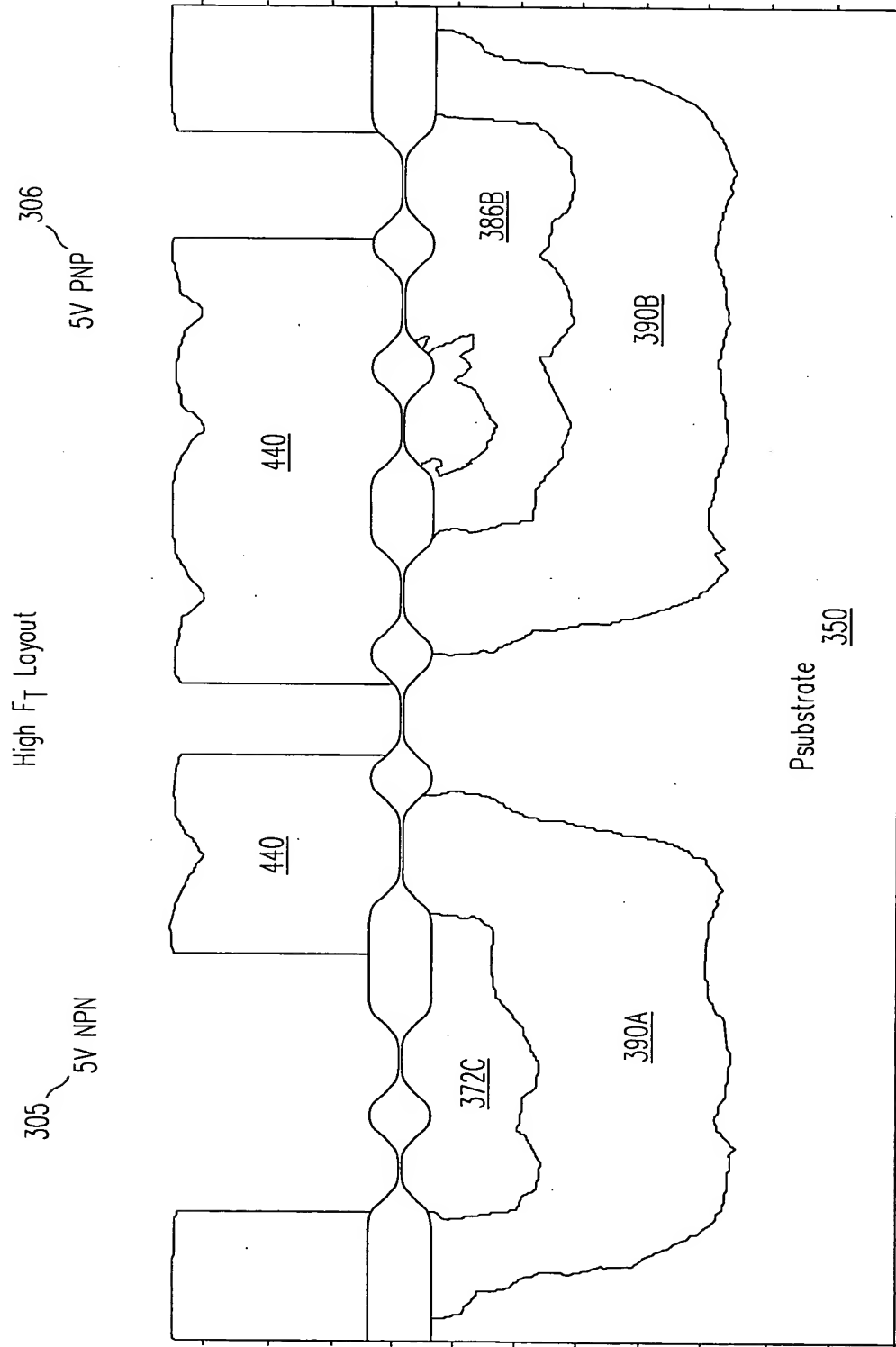
FIG. 44C

FIG. 44E



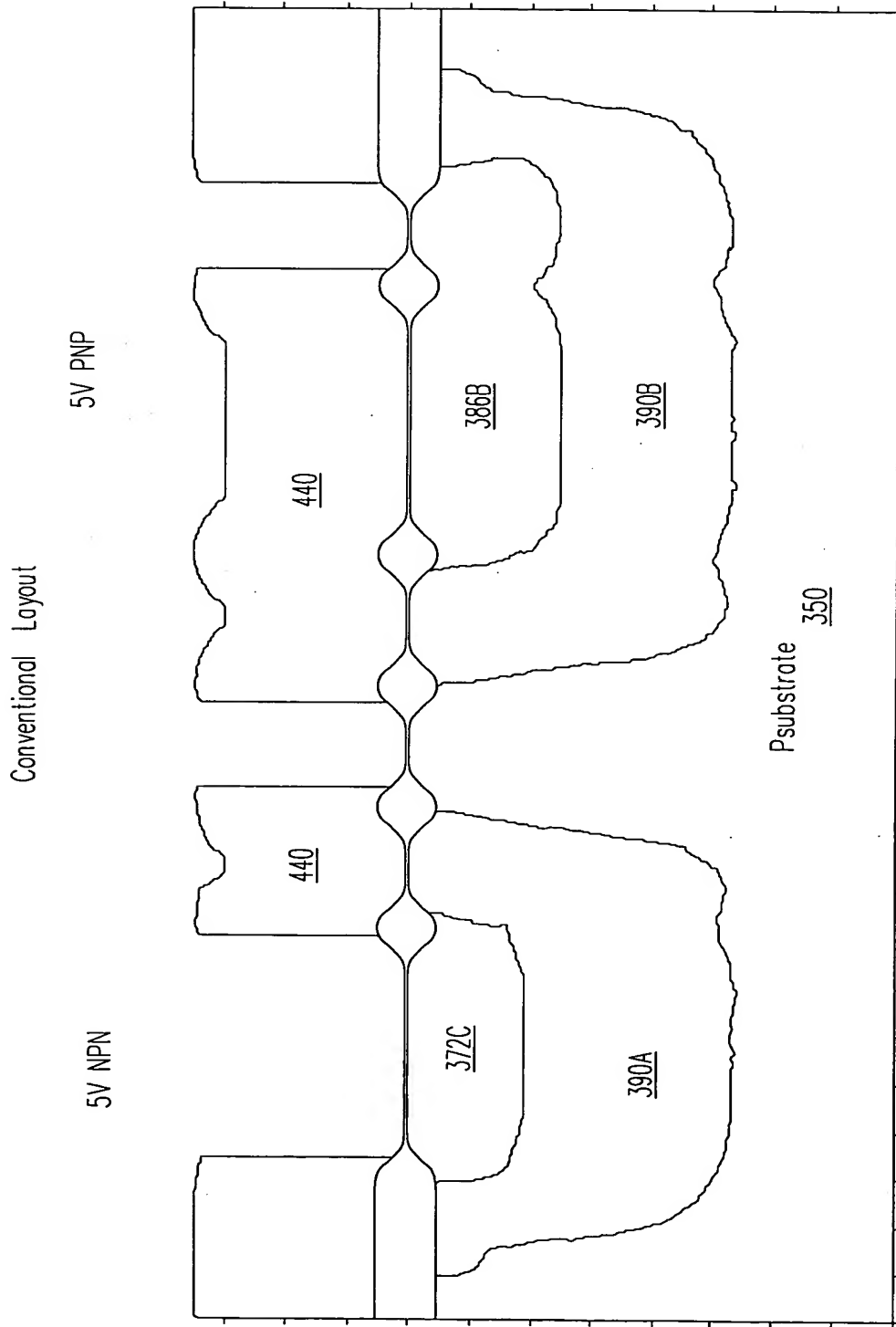
5V P Well Implant-First Stage

FIG. 45A



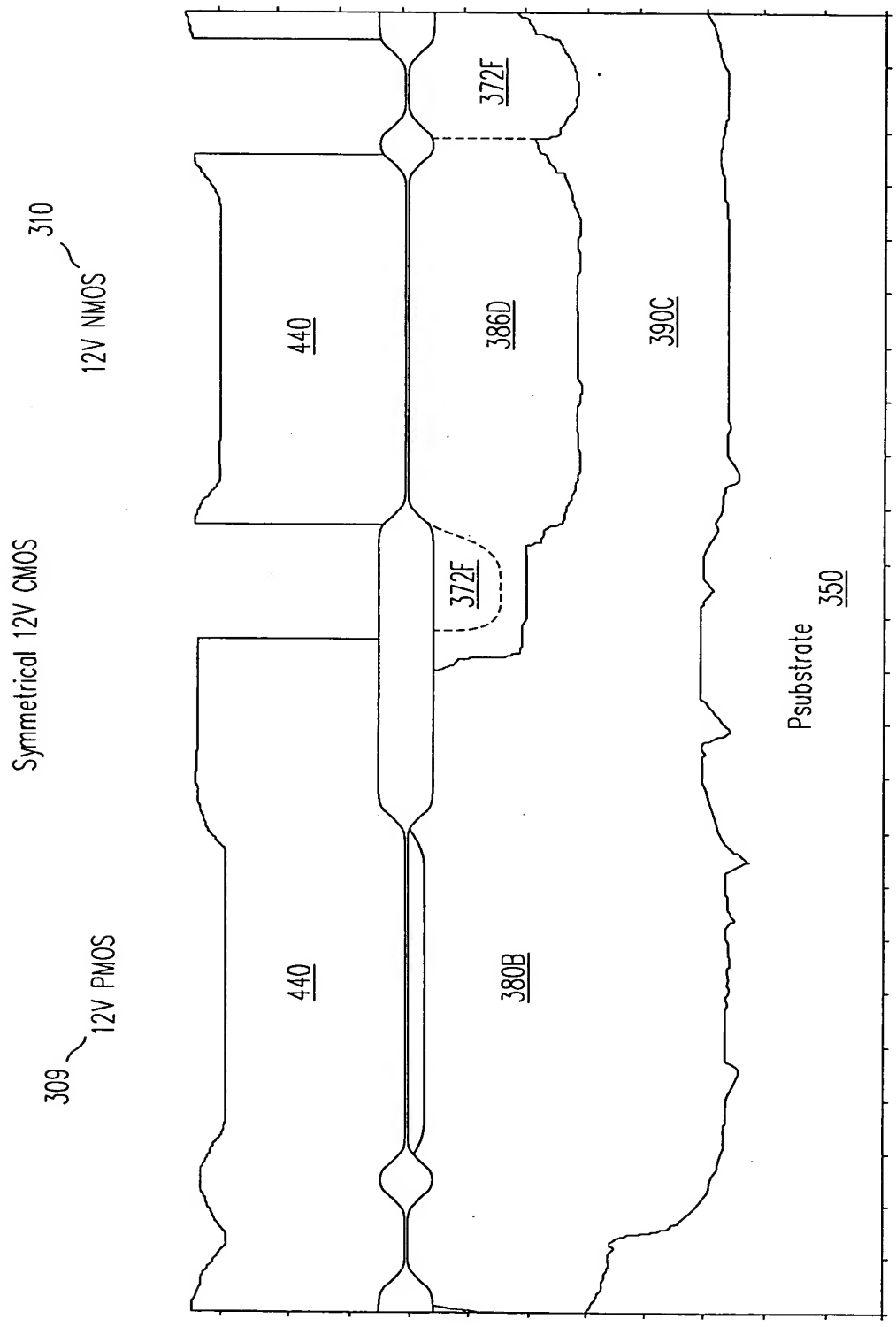
5V P Well Implant-First Stage

FIG. 45B



5V P Well Implant-First Stage

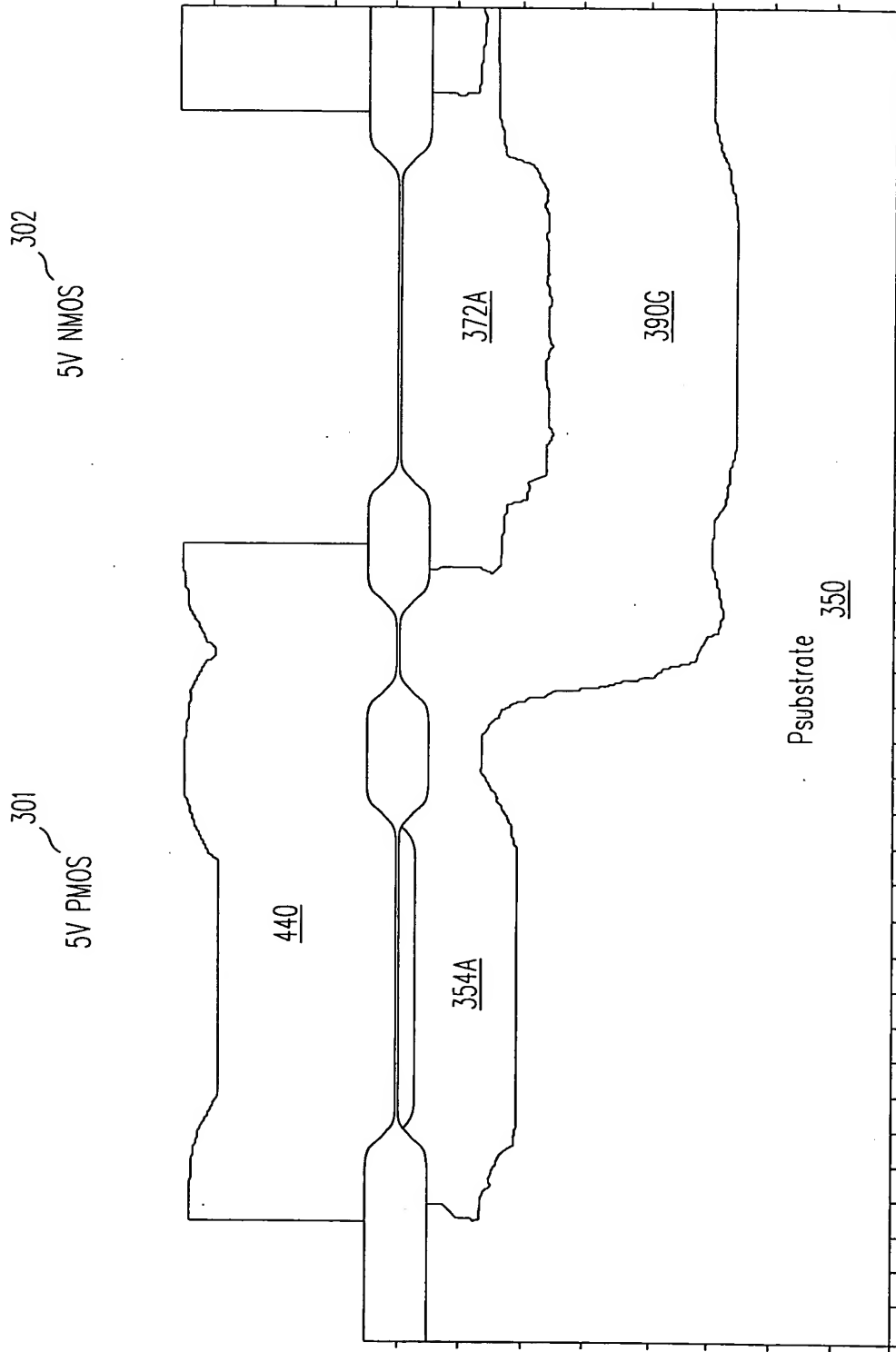
*FIG. 45C*



5V P Well Implant-First Stage

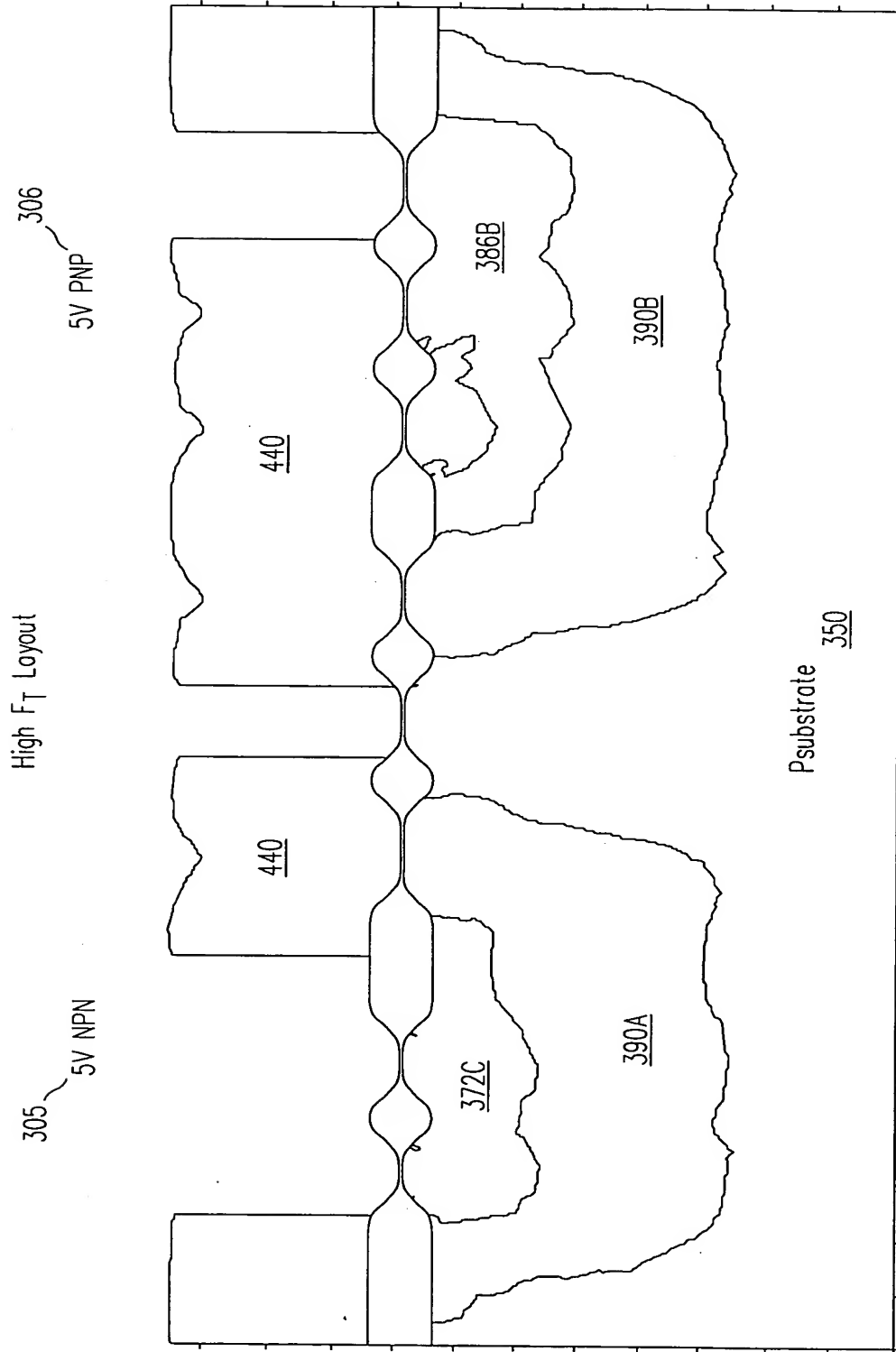
*FIG. 45E*





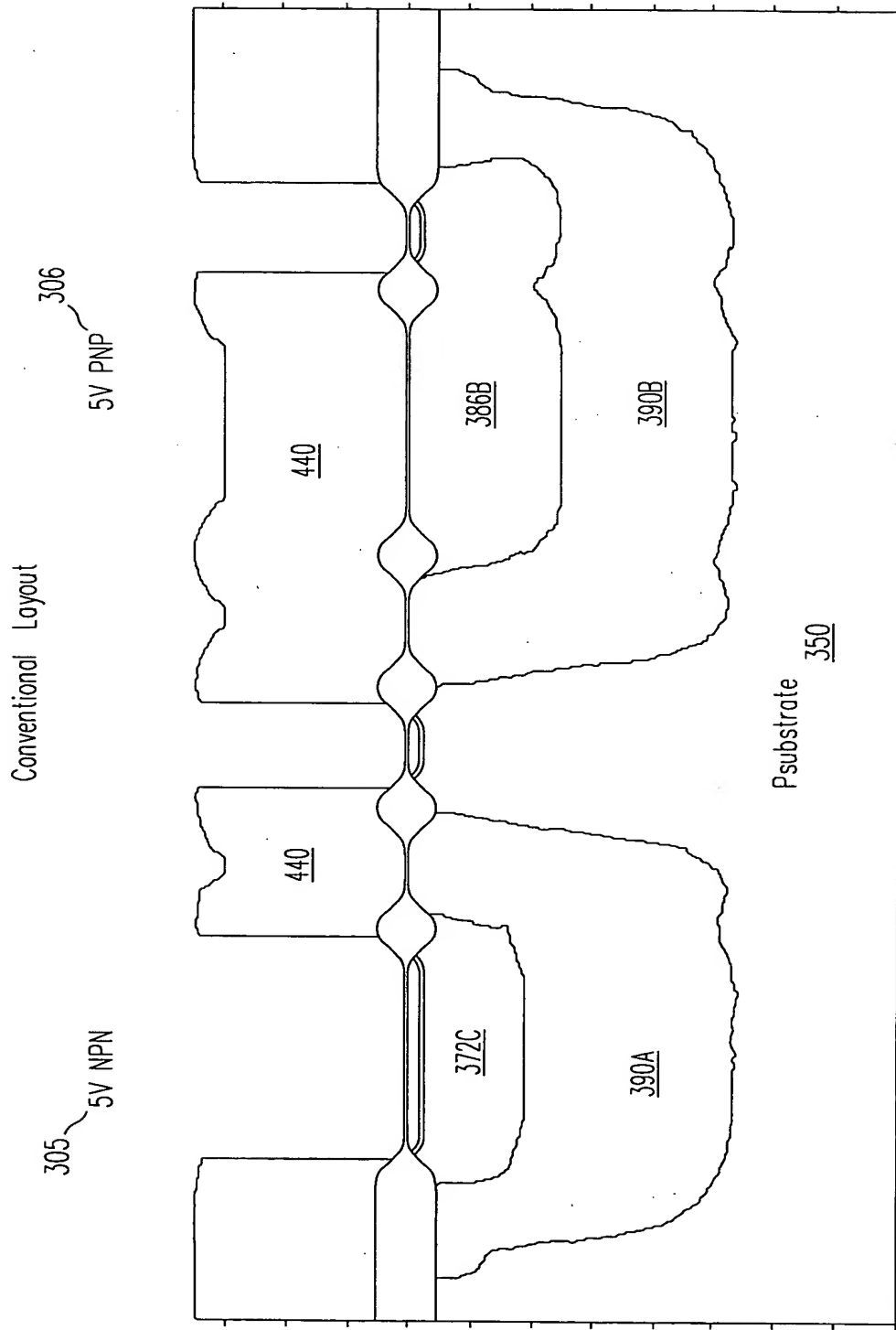
5V P Well Implant-Second Stage

FIG. 46A



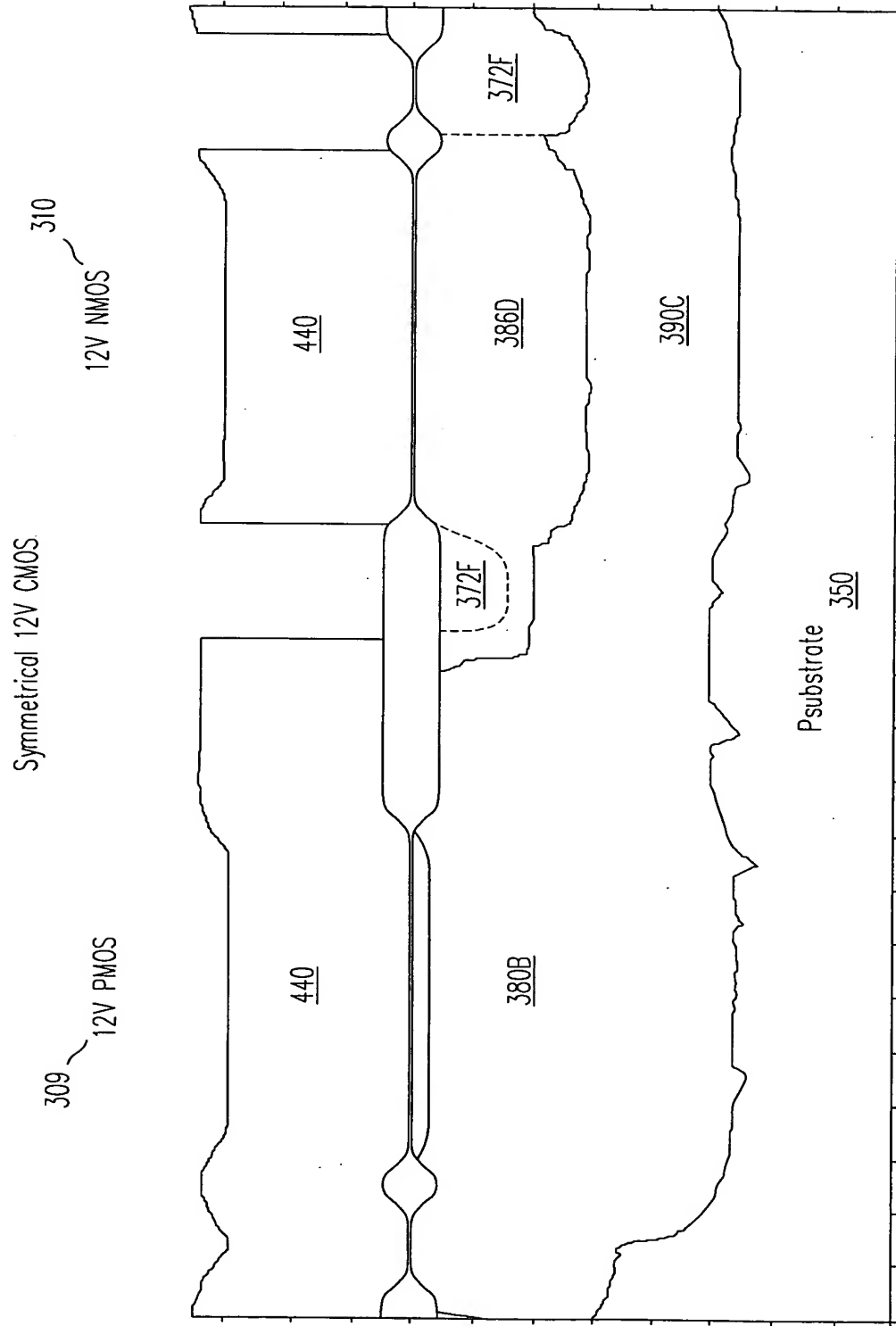
5V P Well Implant-Second Stage

FIG. 46B



5V P Well Implant - Second Stage

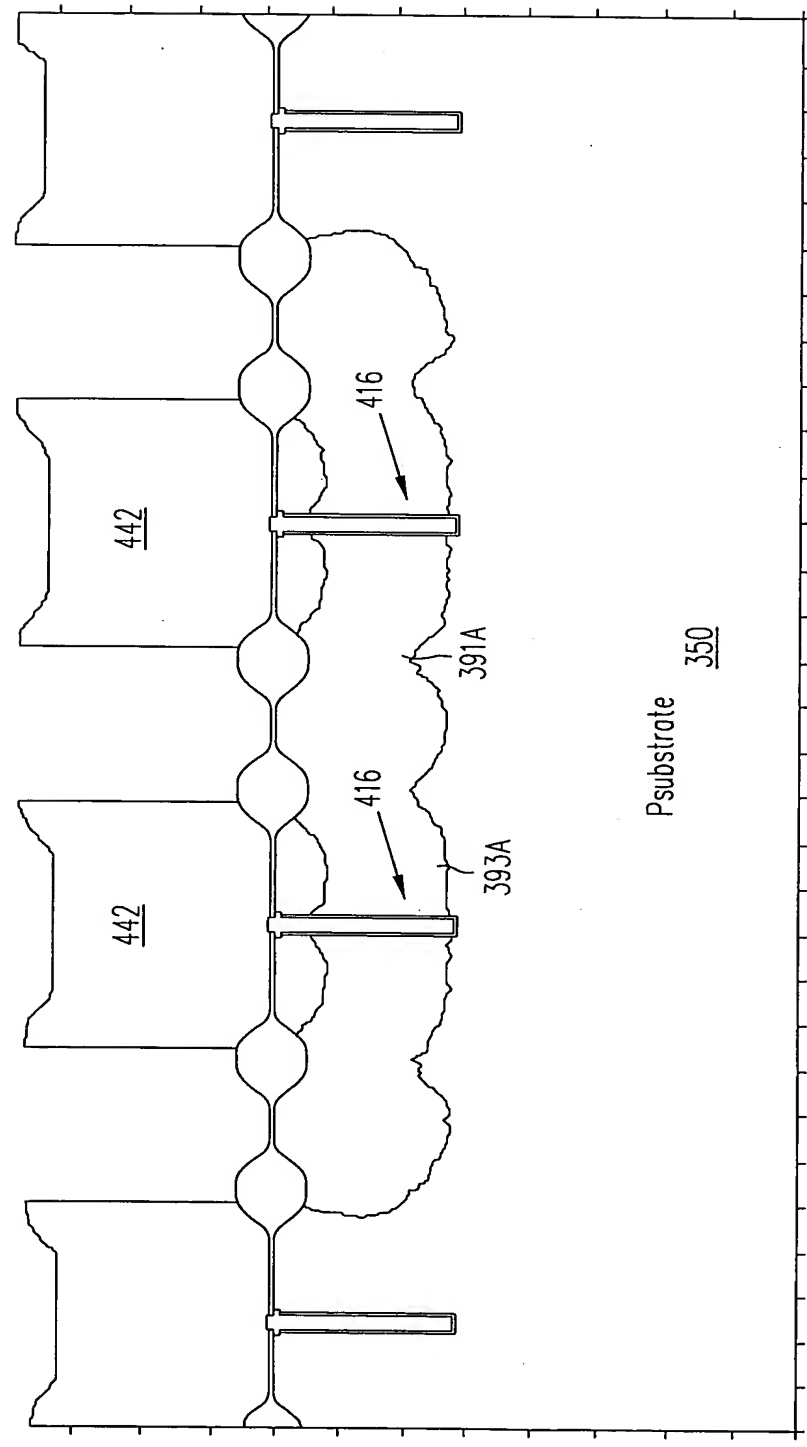
*FIG. 46C*



5V P Well Implant-Second Stage

**FIG. 46E**

30V Lateral Trench DMOS ~ 308



Etch-Block Mask and Etching of Planar Active Regions

FIG. 47D

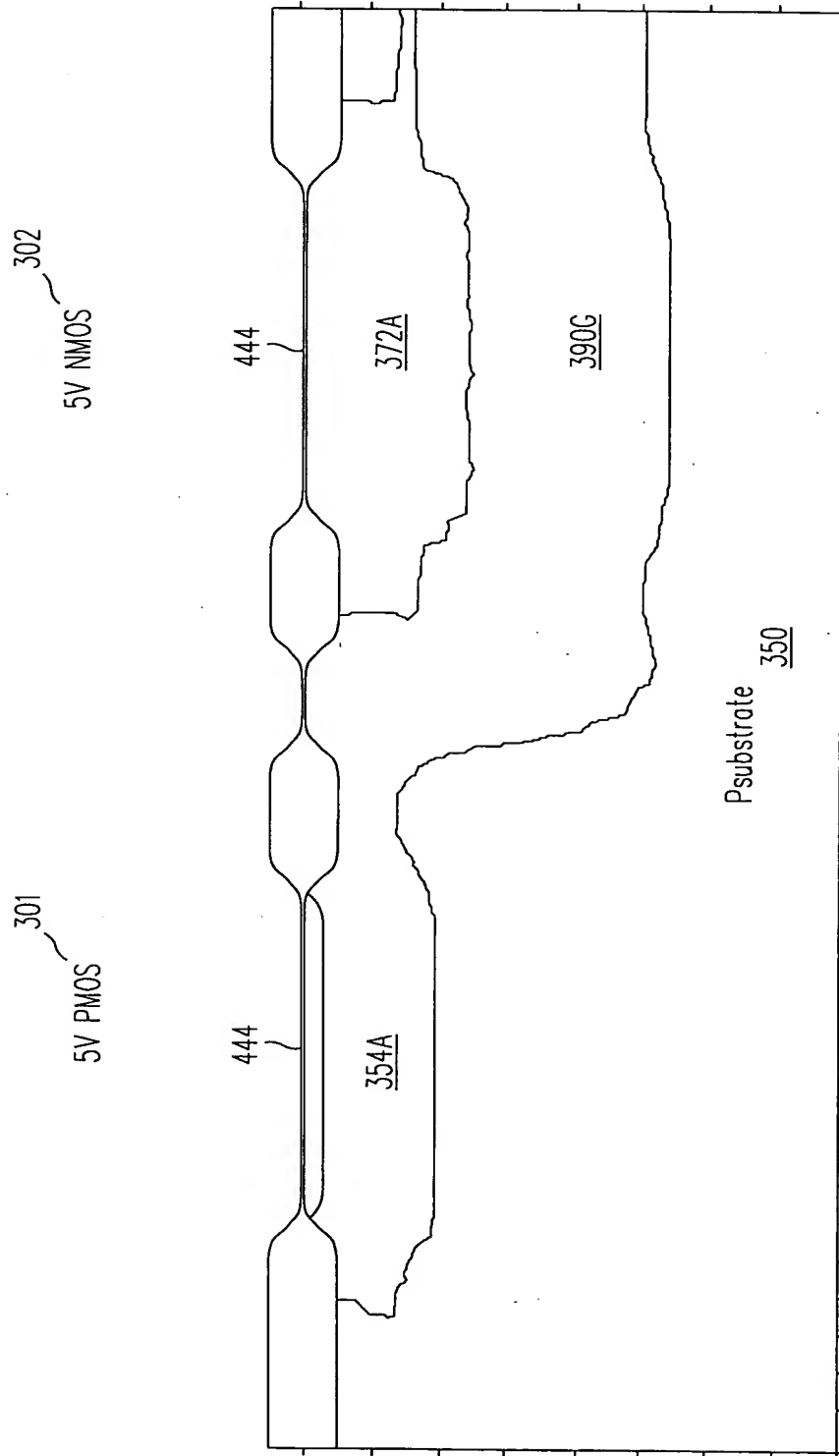
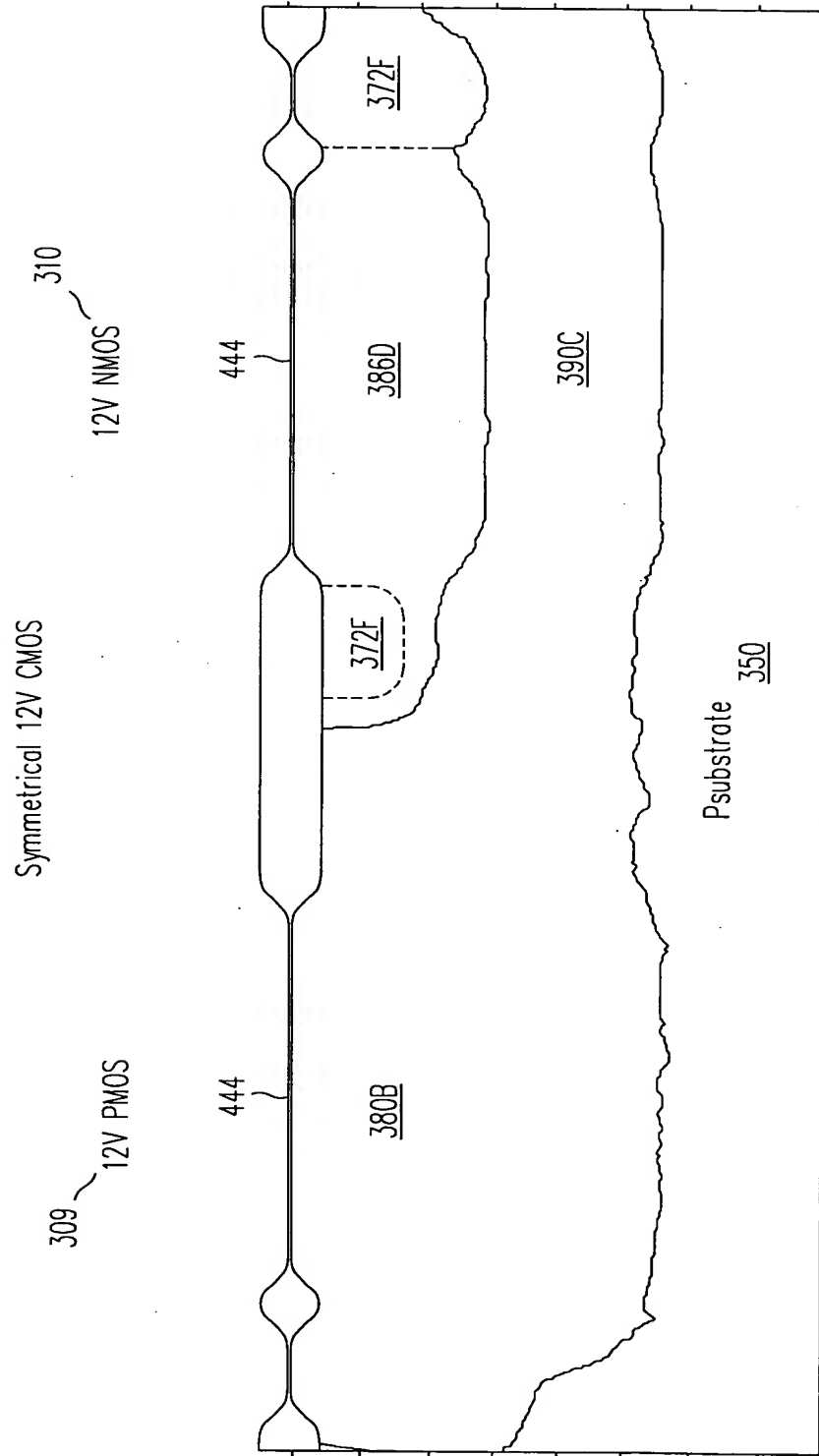
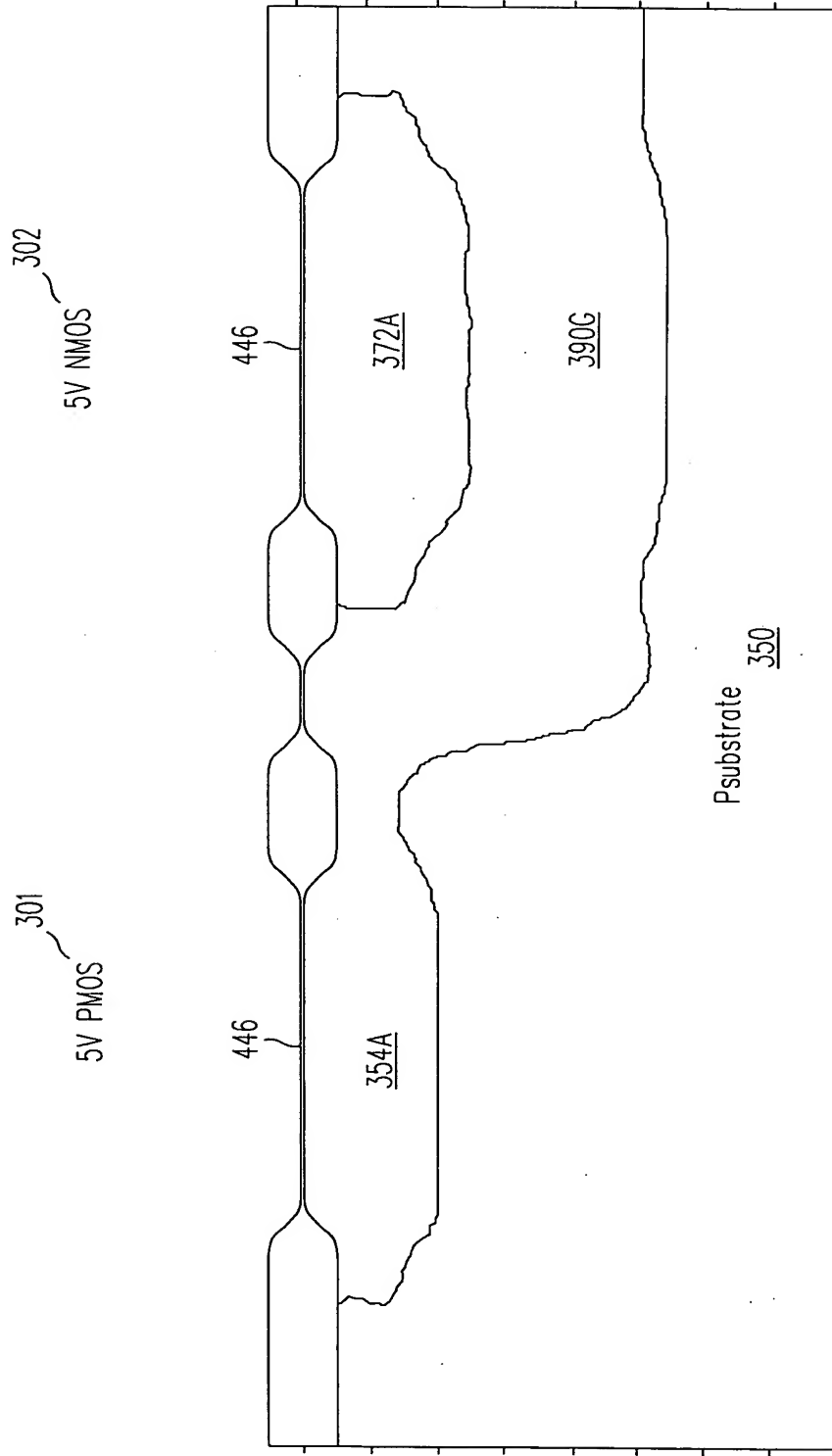


FIG. 48A



First Planar Gate Oxide

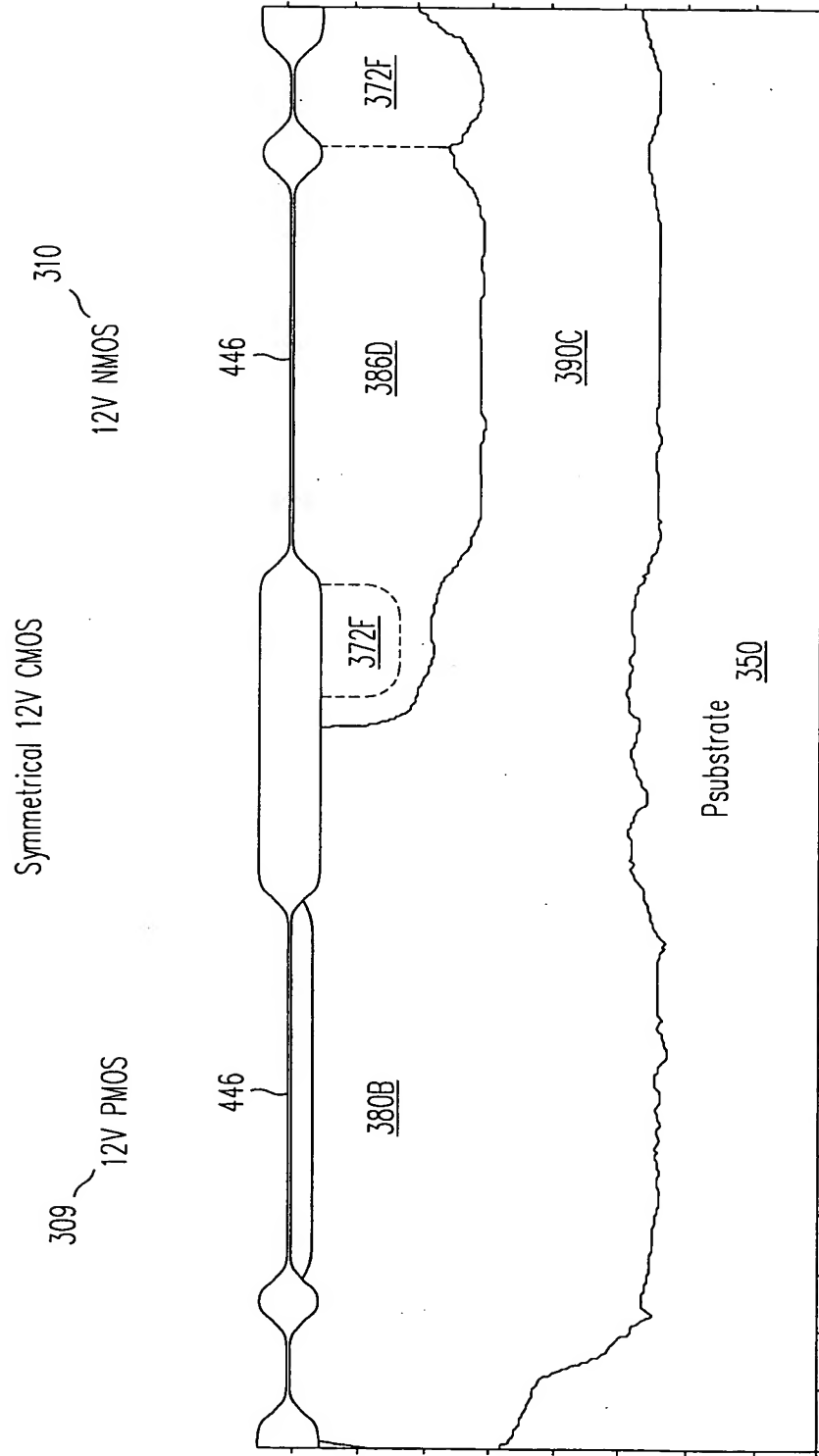
**FIG. 48E**



Threshold Adjust-Implant-First Stage

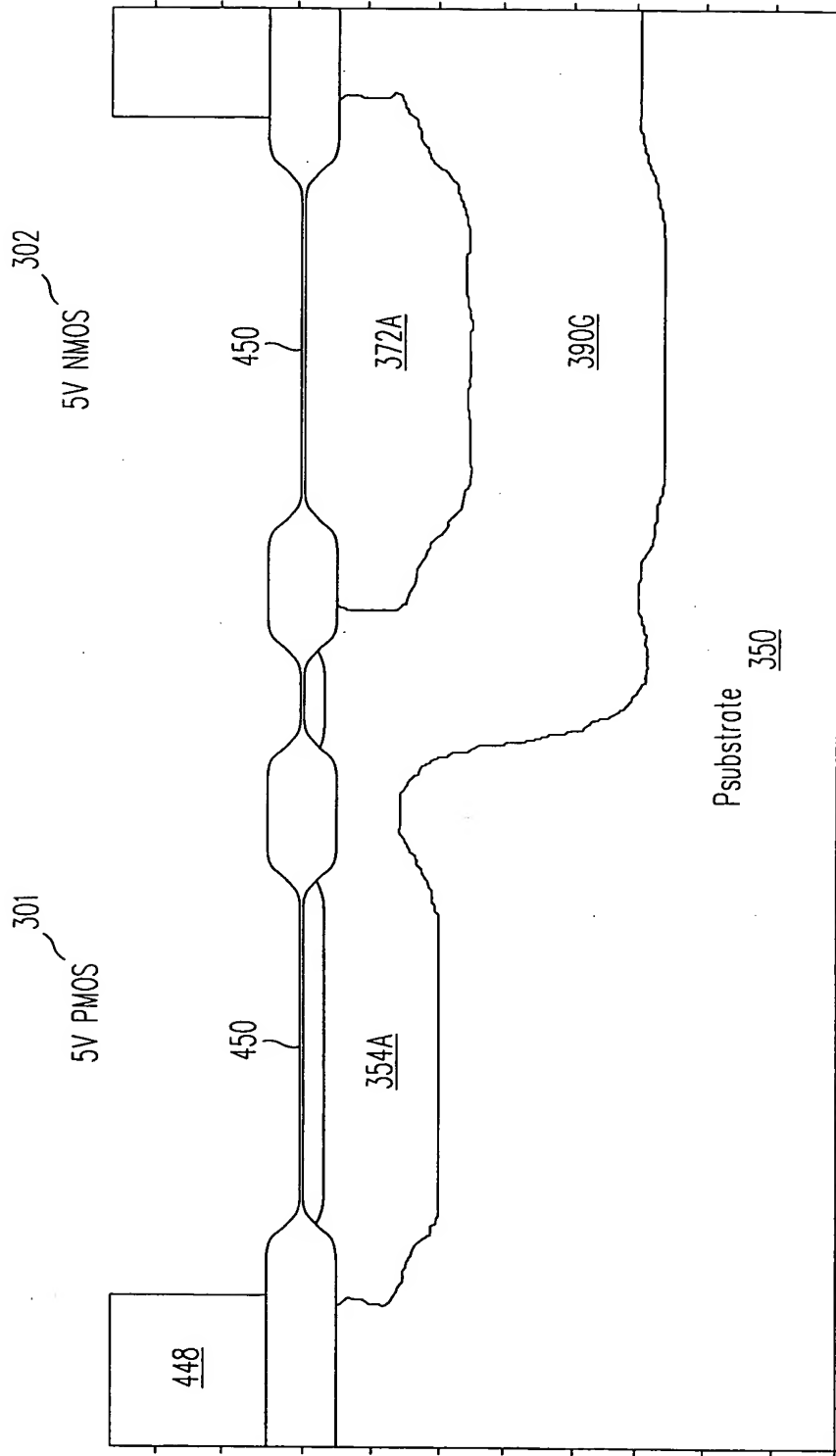
FIG. 49A





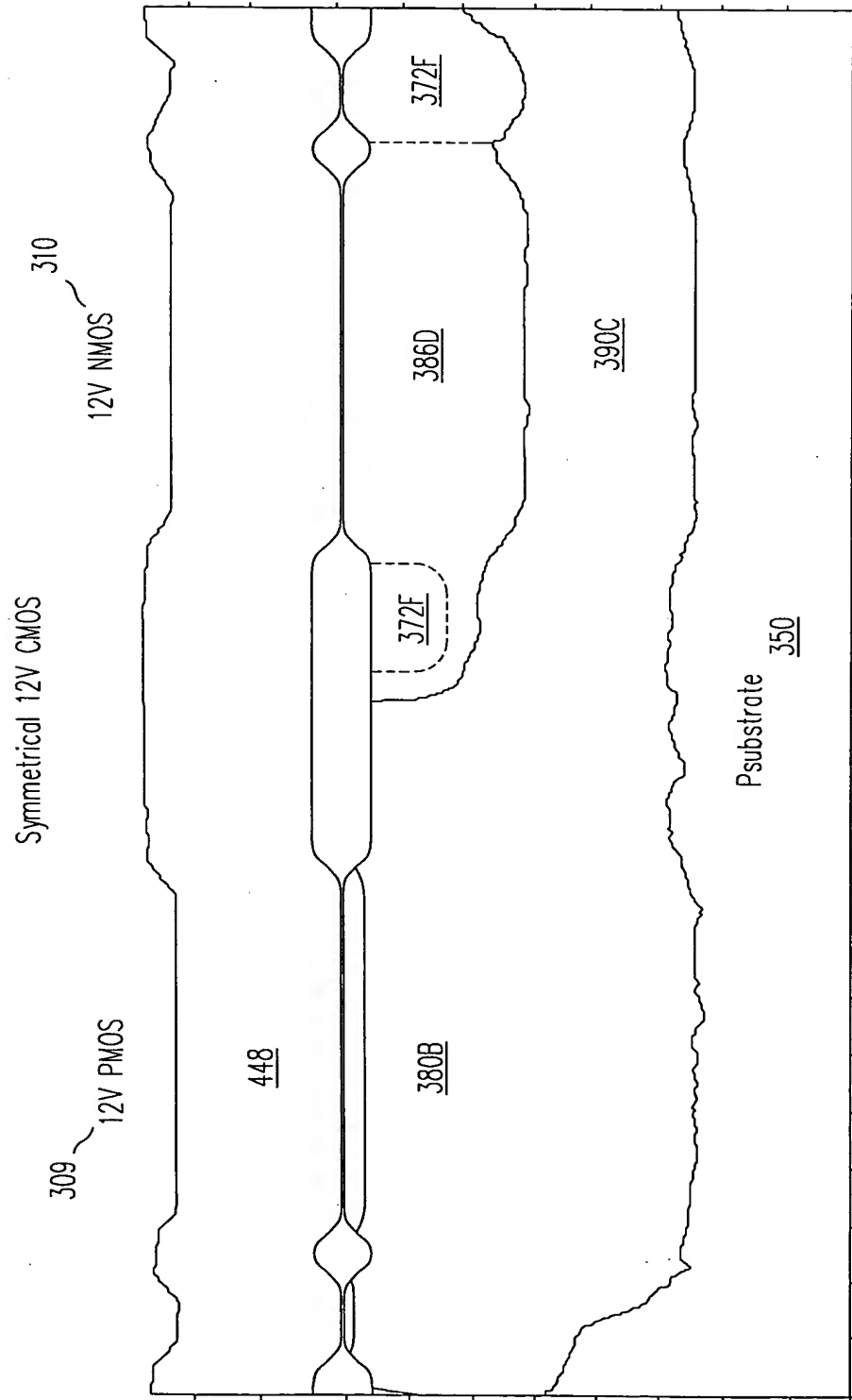
Threshold Adjust Implant-First Stage

FIG. 49E



Threshold Adjust Implant-Second Stage  
First Planar Gate Oxide Removal

FIG. 50A



Threshold Adjust Implant-Second Stage

FIG. 50E

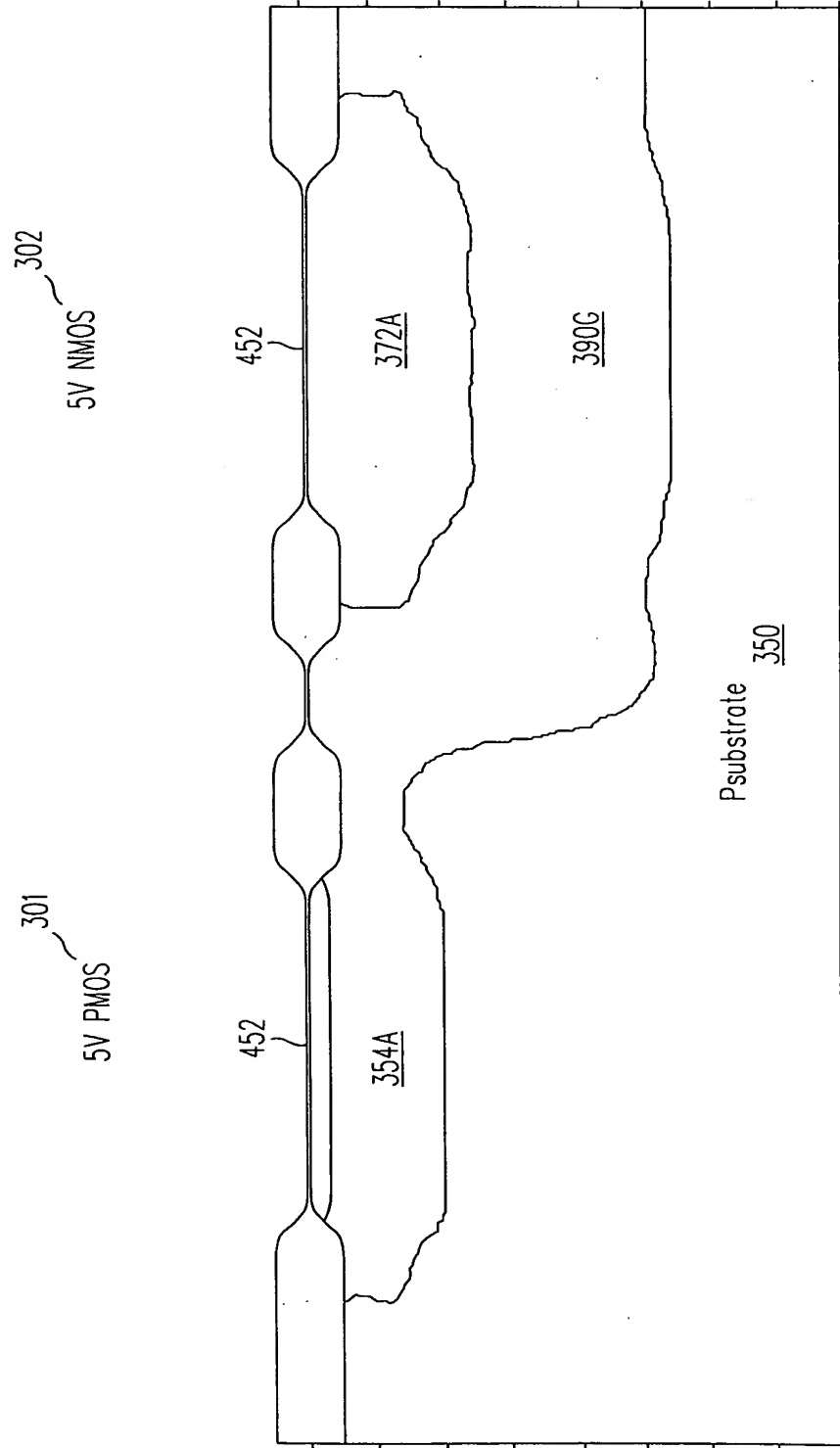
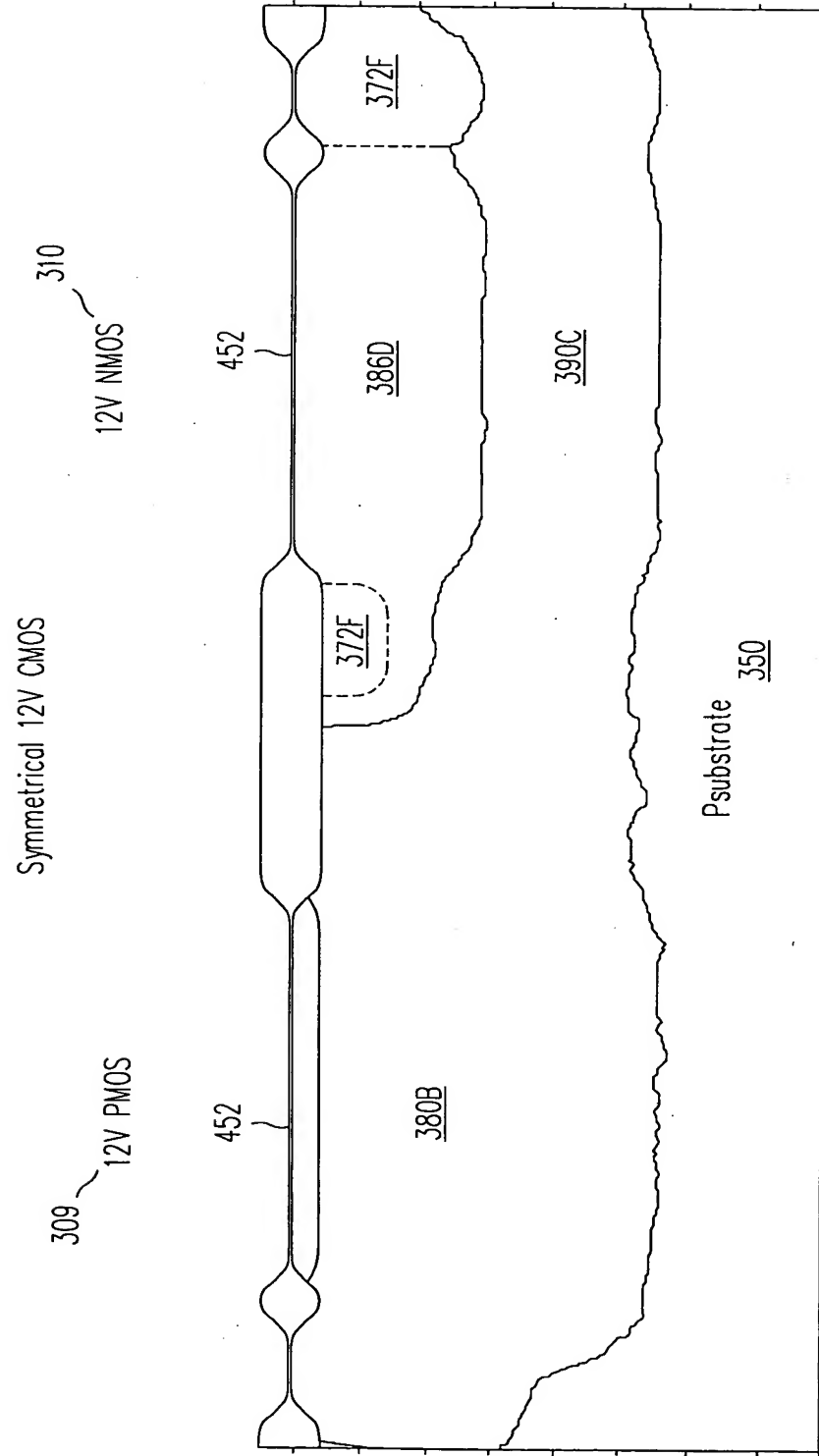


FIG. 51A



Second Planar Gate Oxide

FIG. 51E

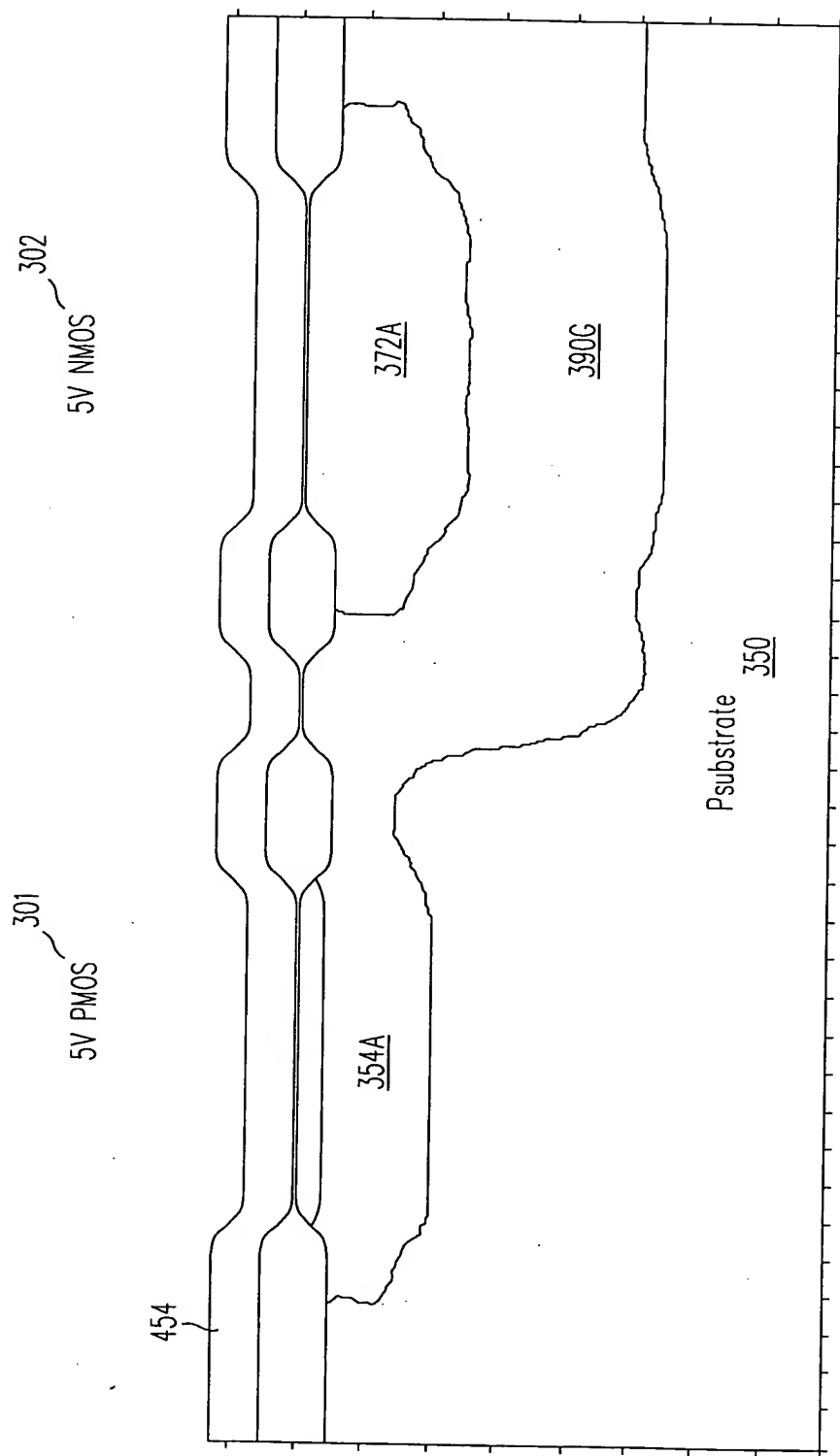
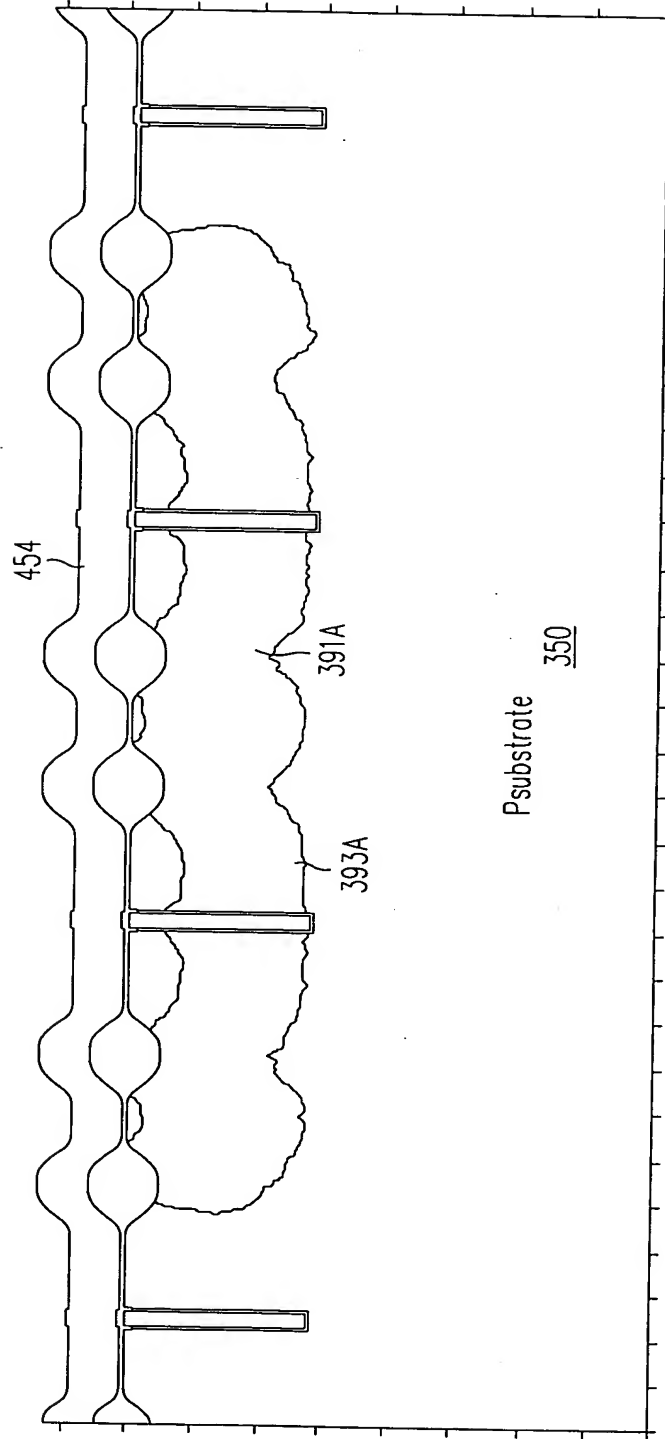


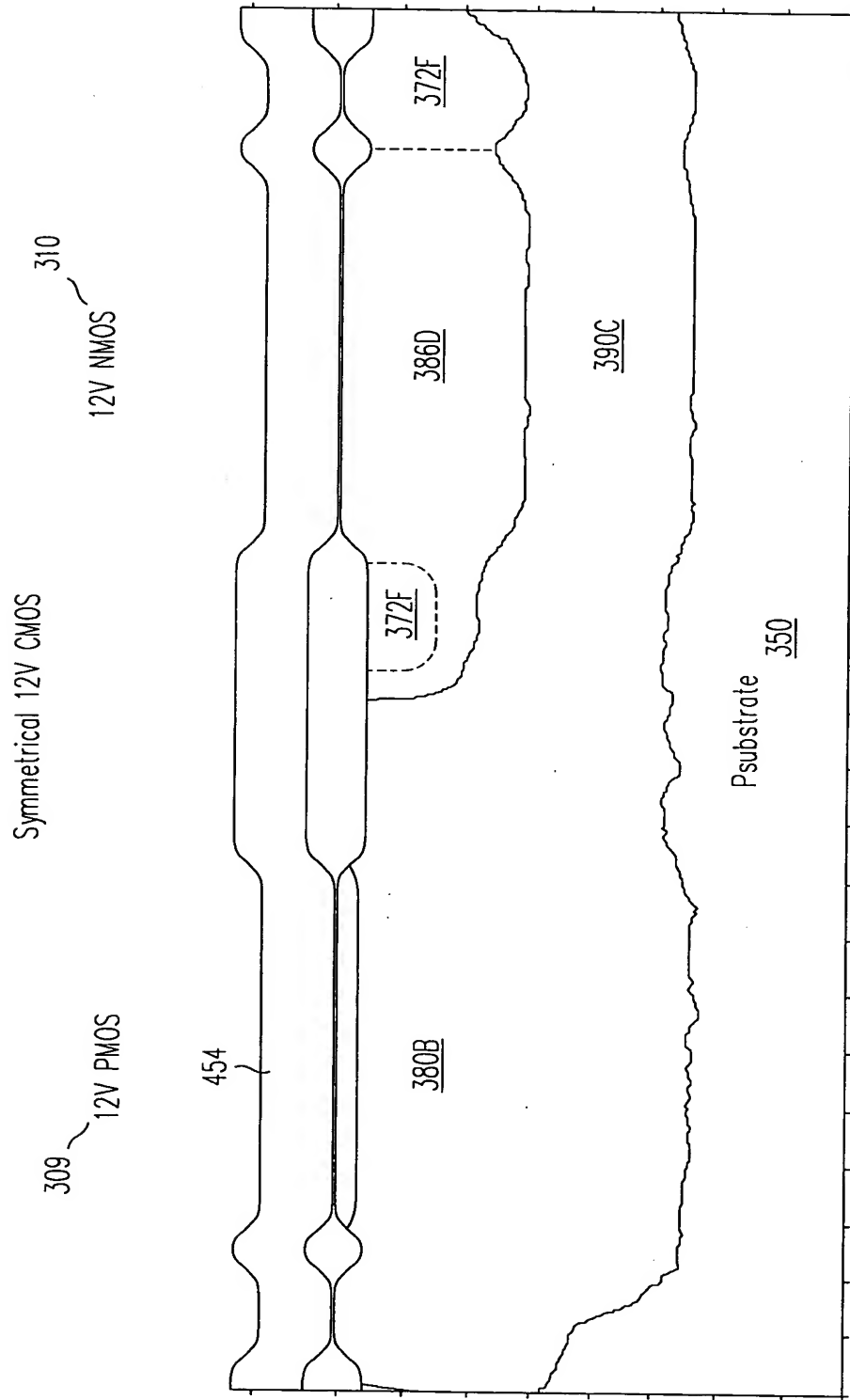
FIG. 52A

30V Lateral Trench DMOS ~ 308



Polysilicon-Third Layer

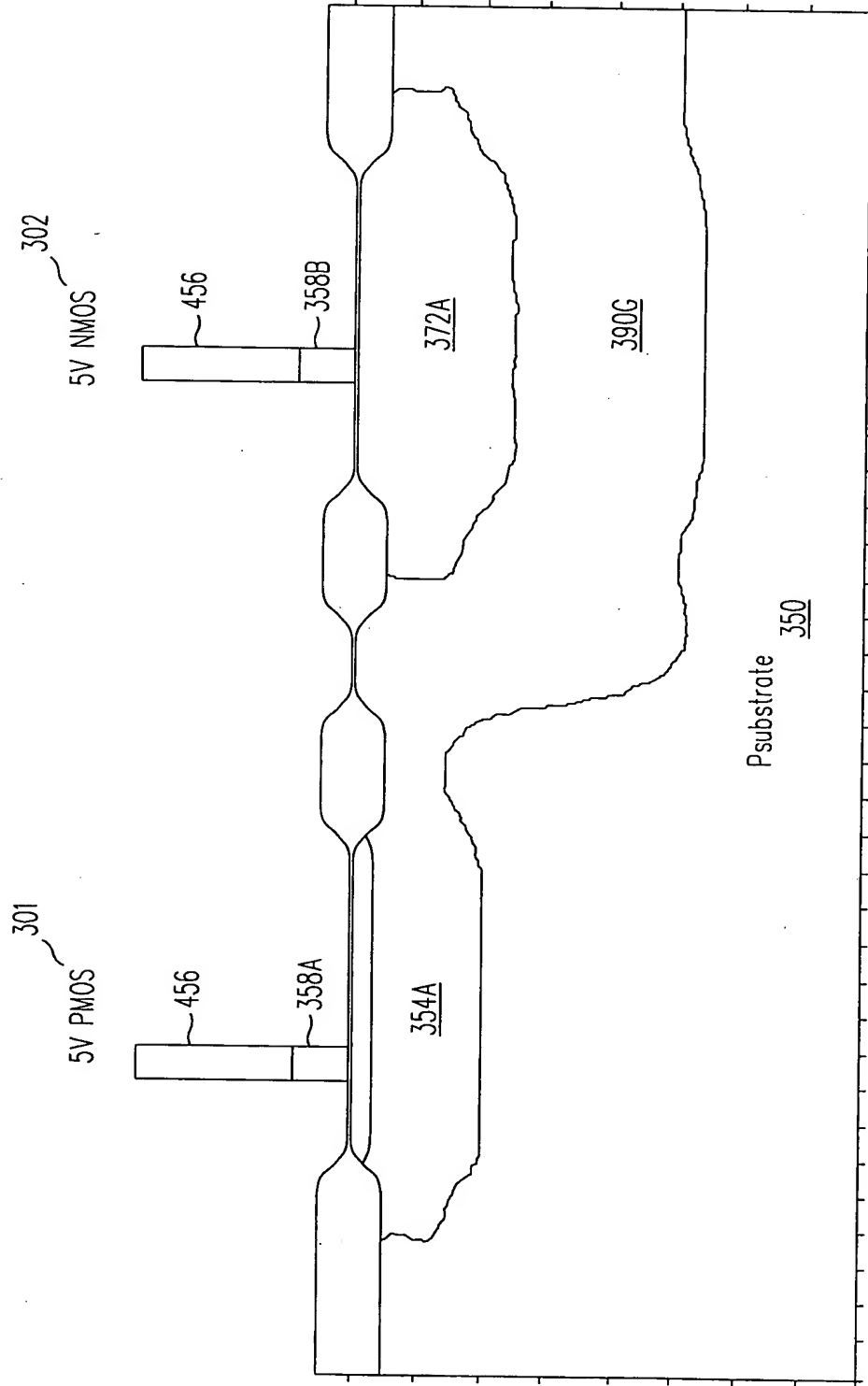
FIG. 52D



Polysilicon—Third Layer

*FIG. 52E*

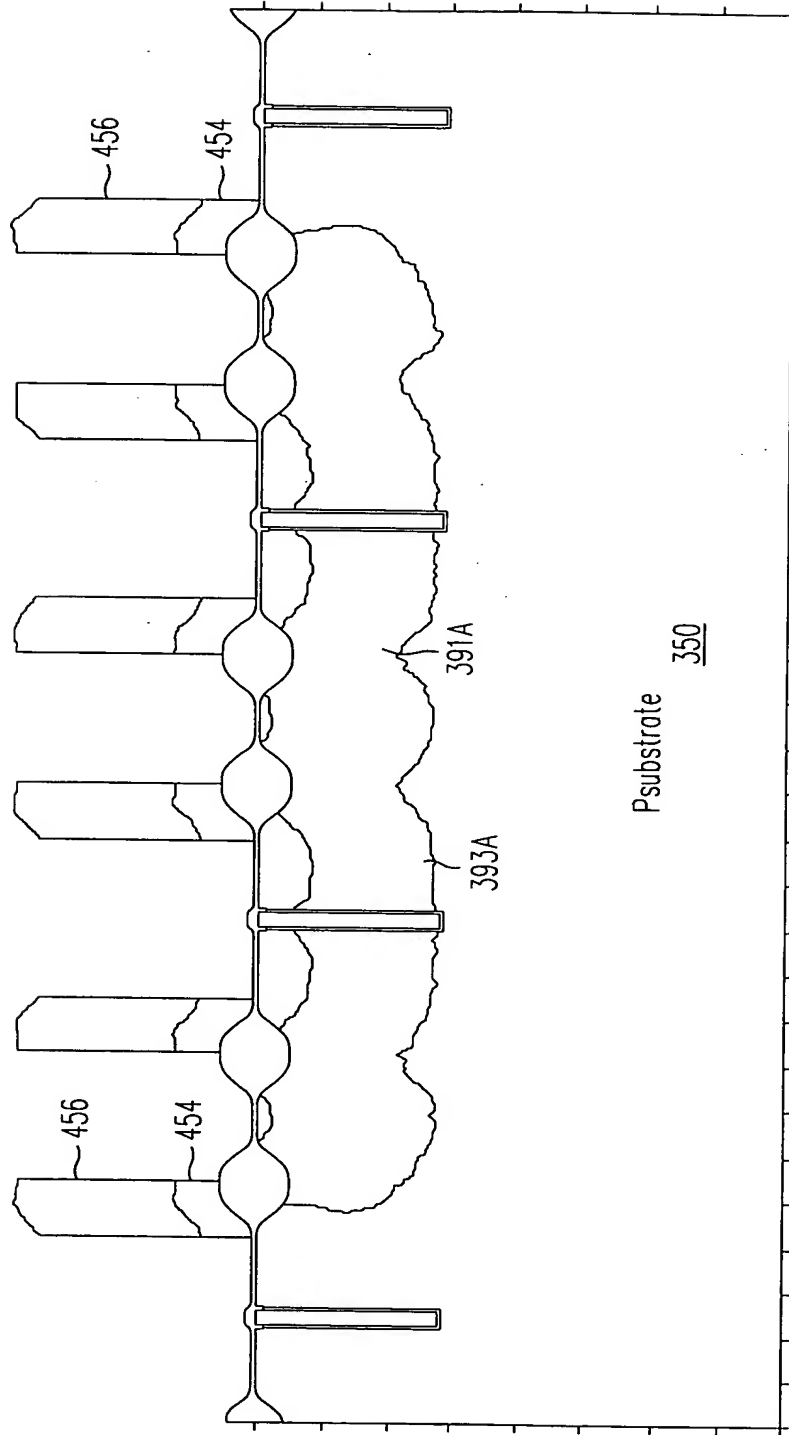




Planar Gate Formation

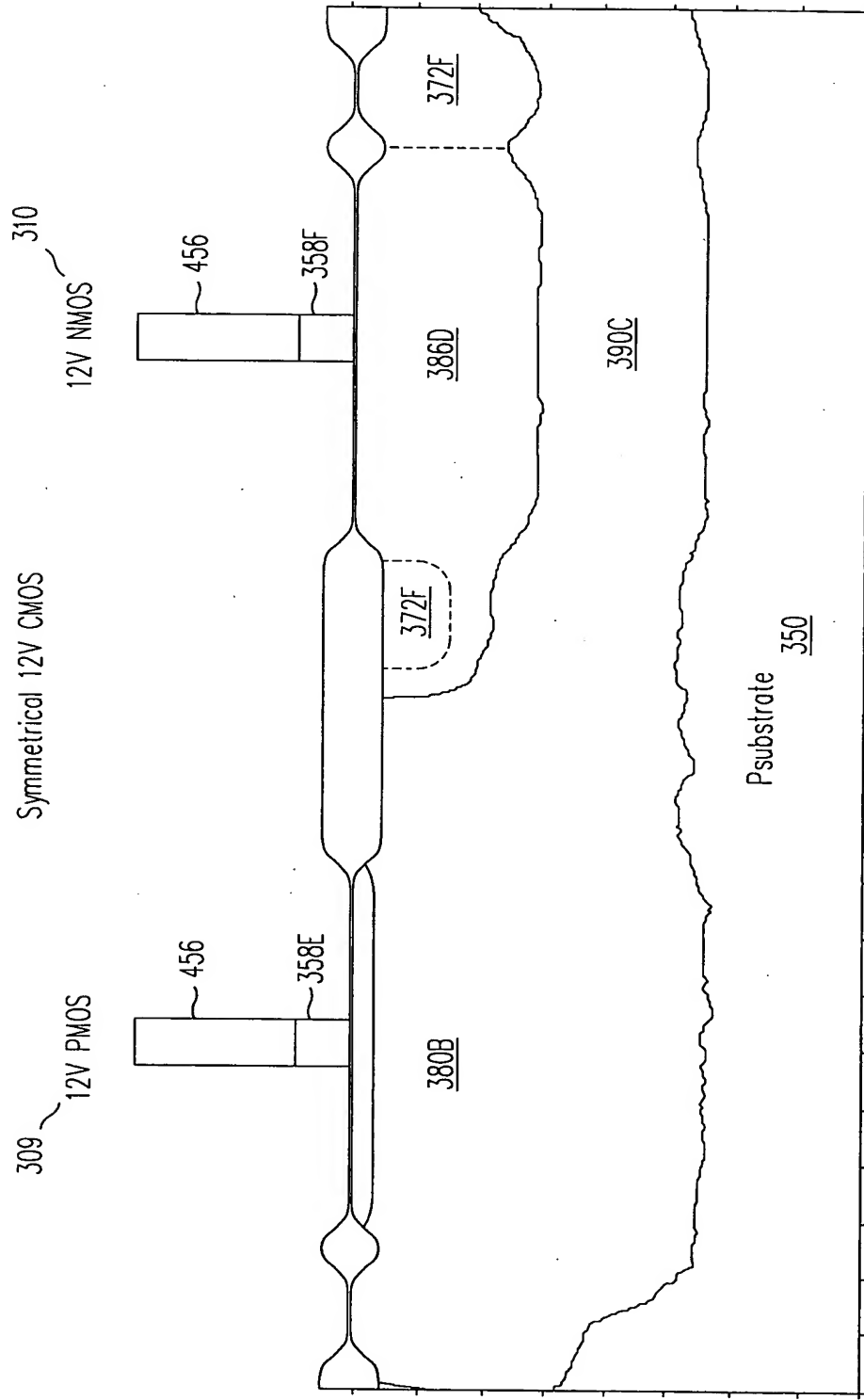
**FIG. 53A**

30V Lateral Trench DMOS ~ 308



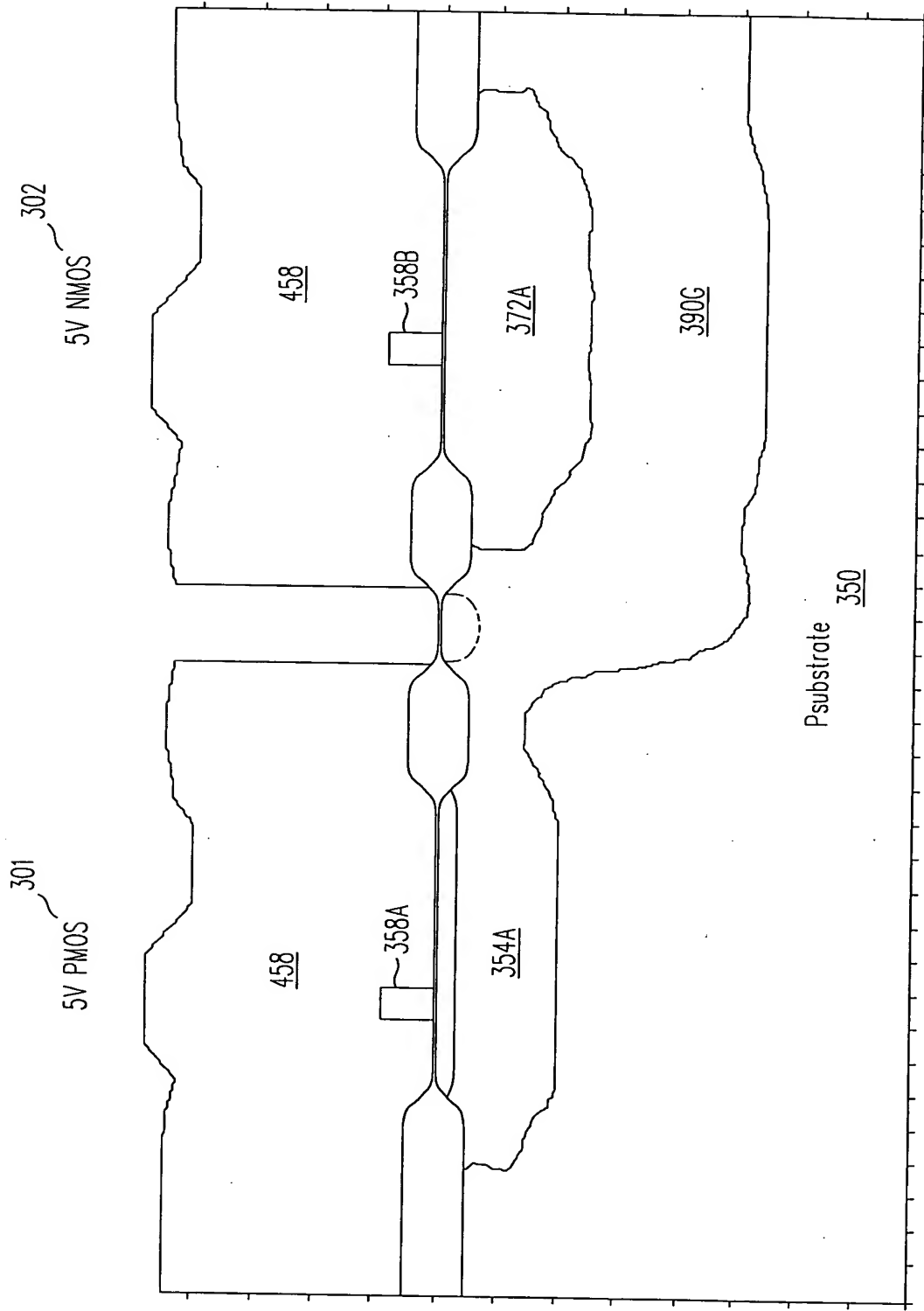
Planar Gate Formation

FIG. 53D



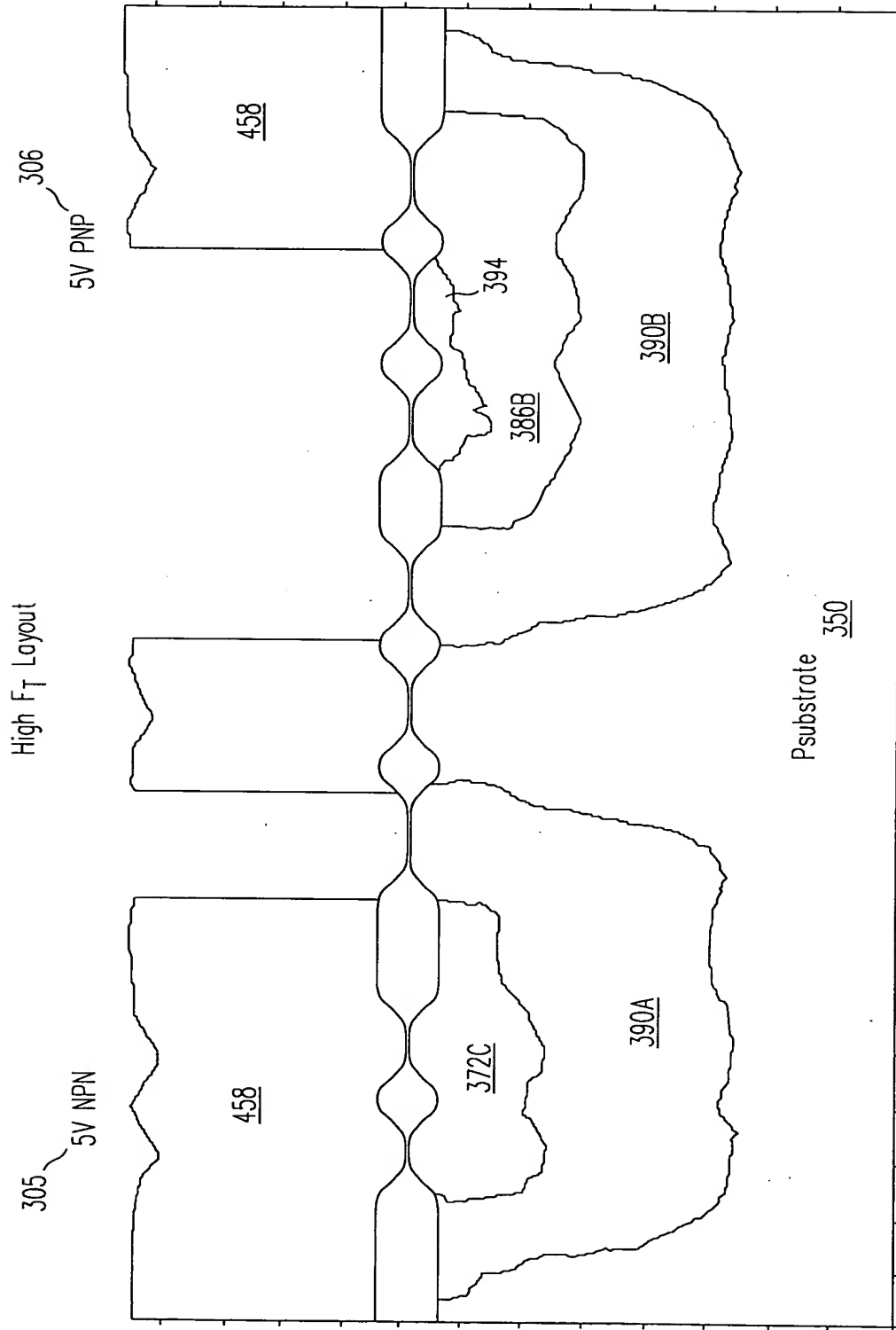
Planar Gate Formation

**FIG. 53E**



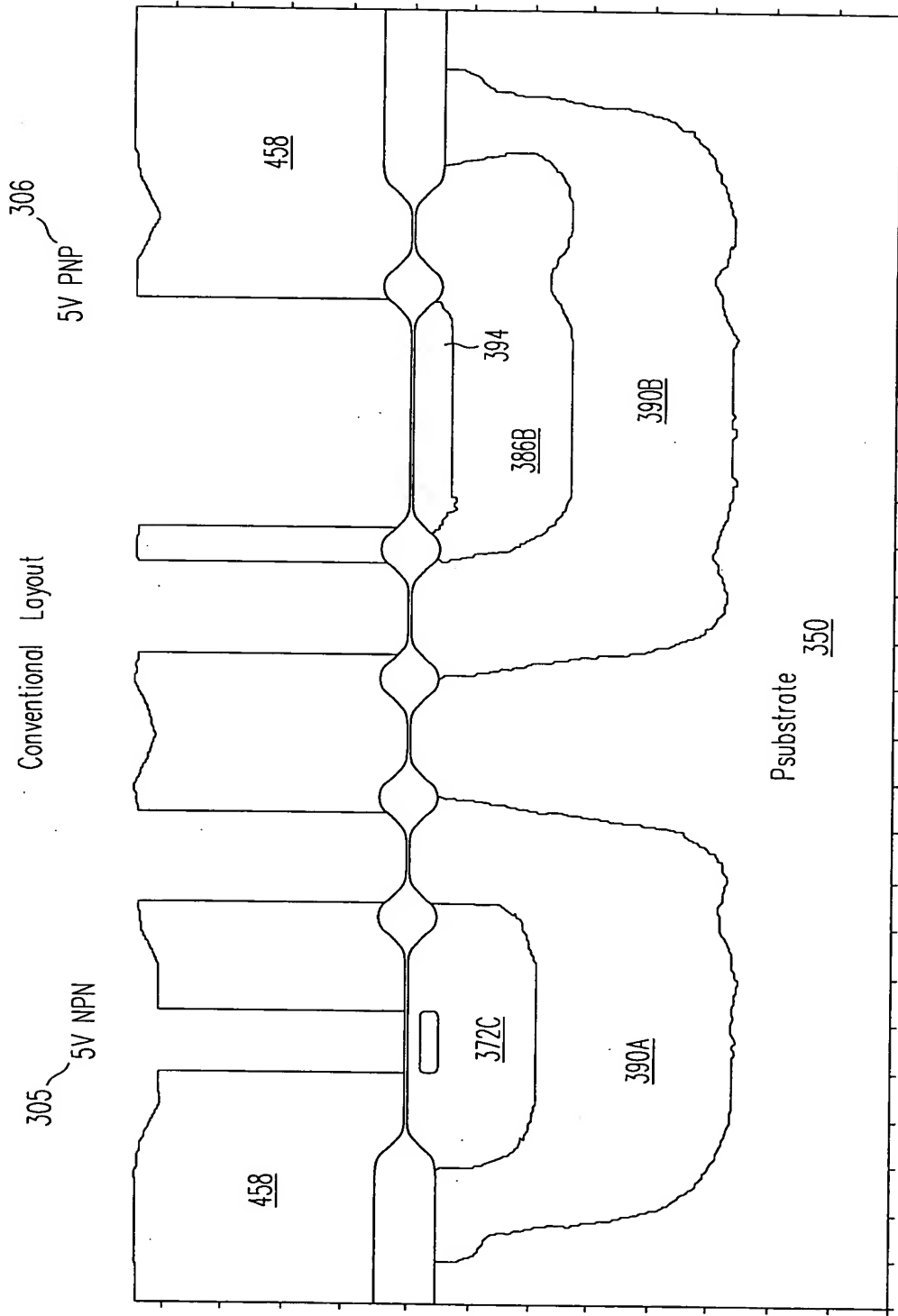
N-Base Mask and Implant

**FIG. 54A**



N-Base Mask and Implant

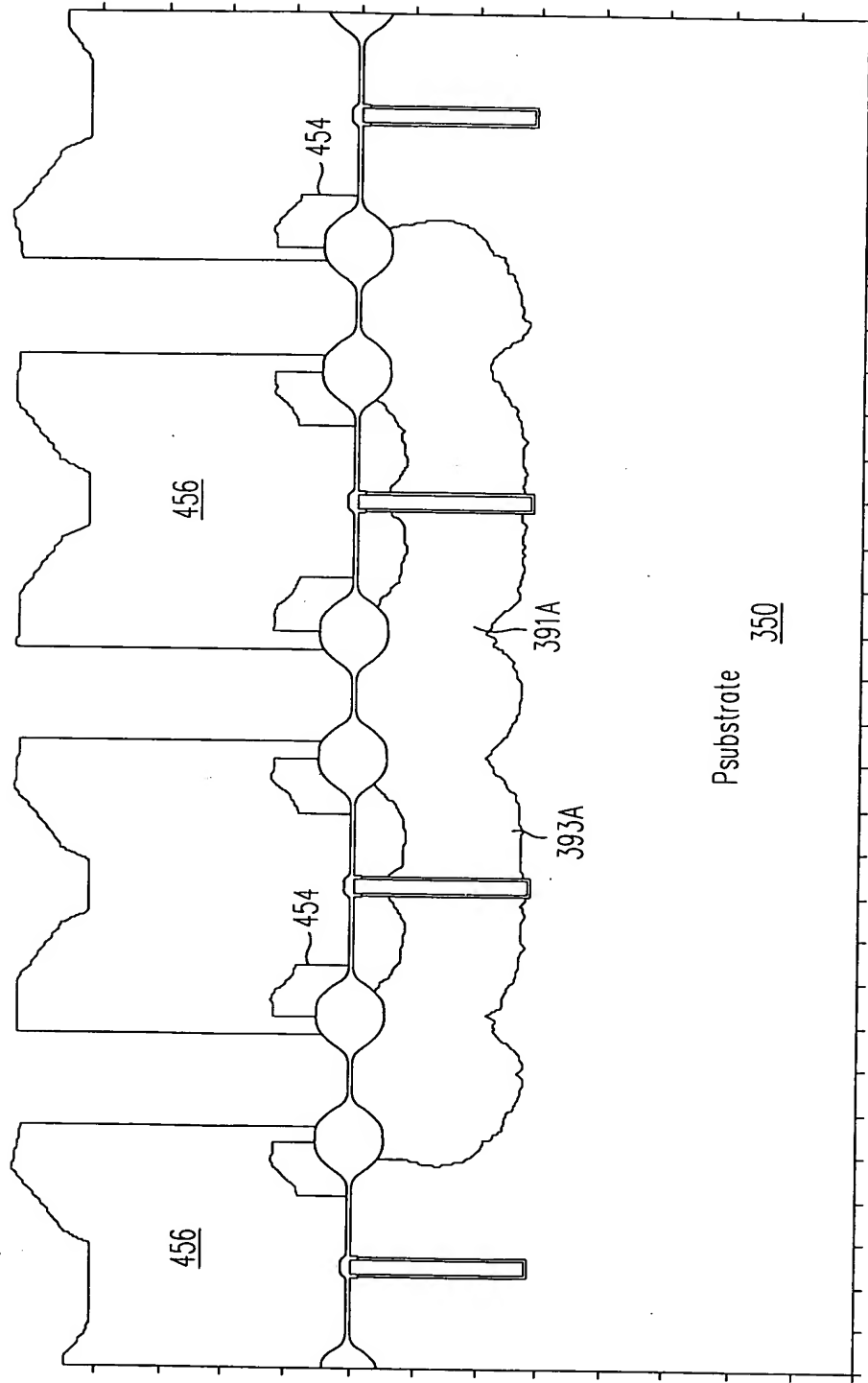
**FIG. 54B**



N-Base Mask and Implant

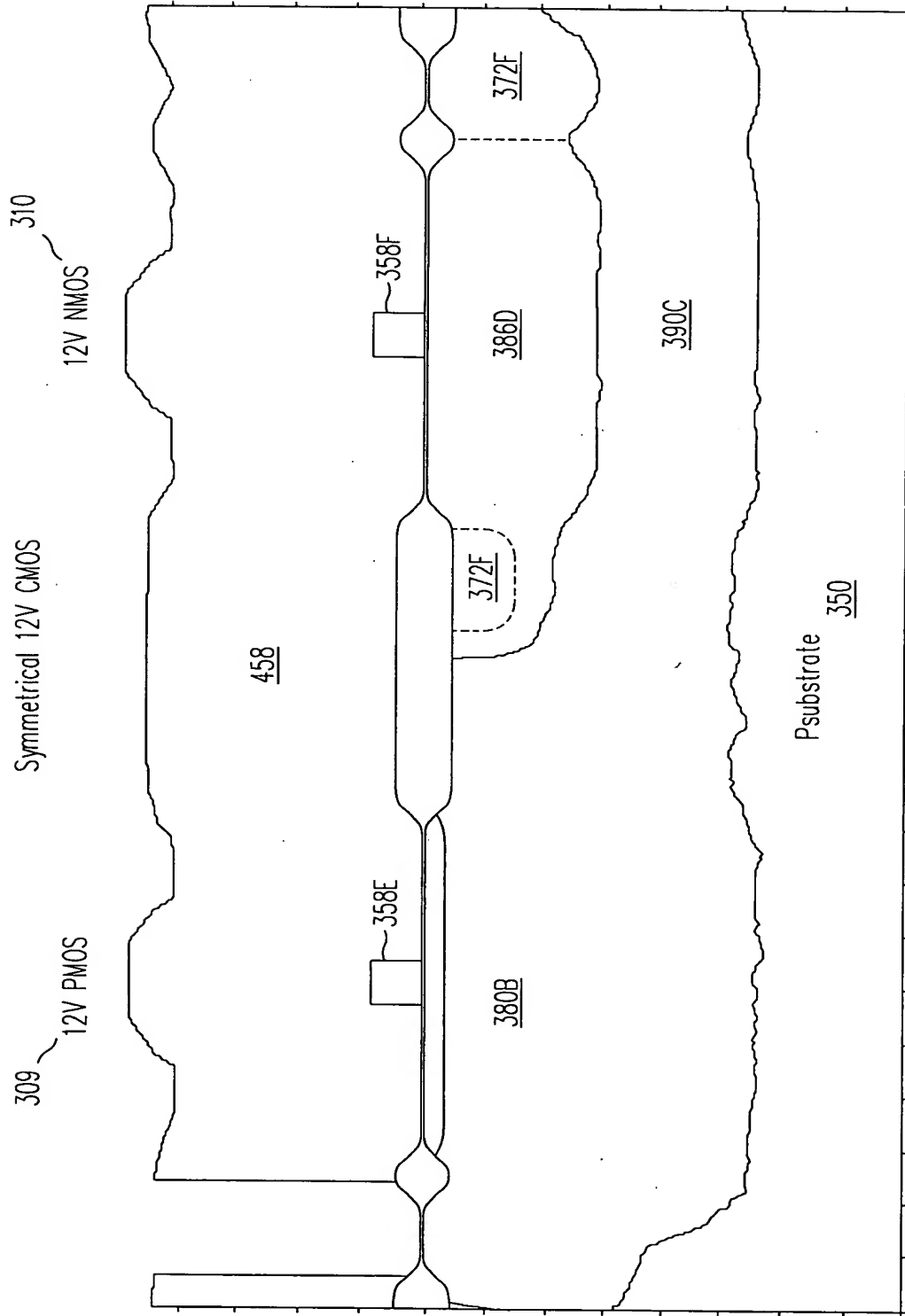
*FIG. 54C*

30V Lateral Trench DMOS ~ 308



N-Base Mask and Implant

*FIG. 54D*

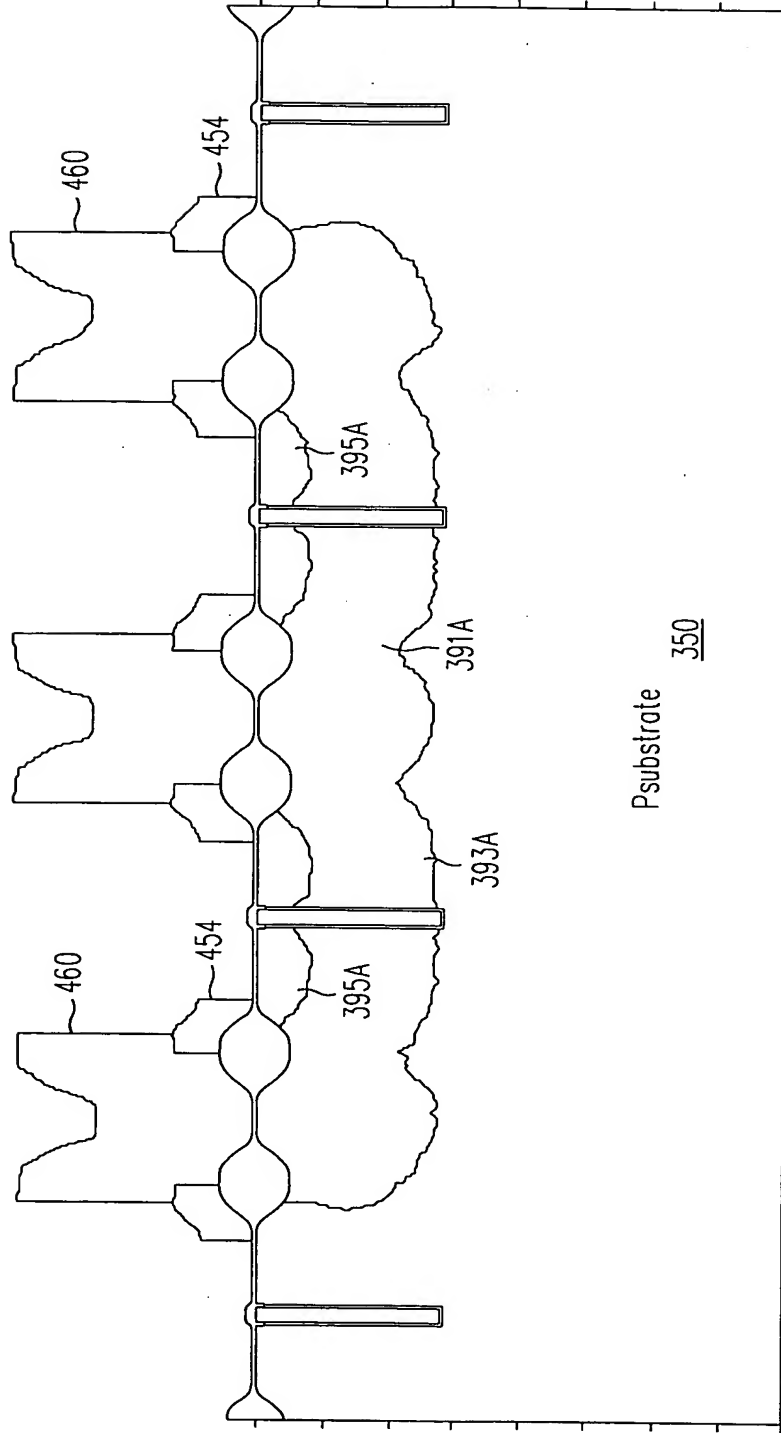


N-Base Mask and Implant

FIG. 54E



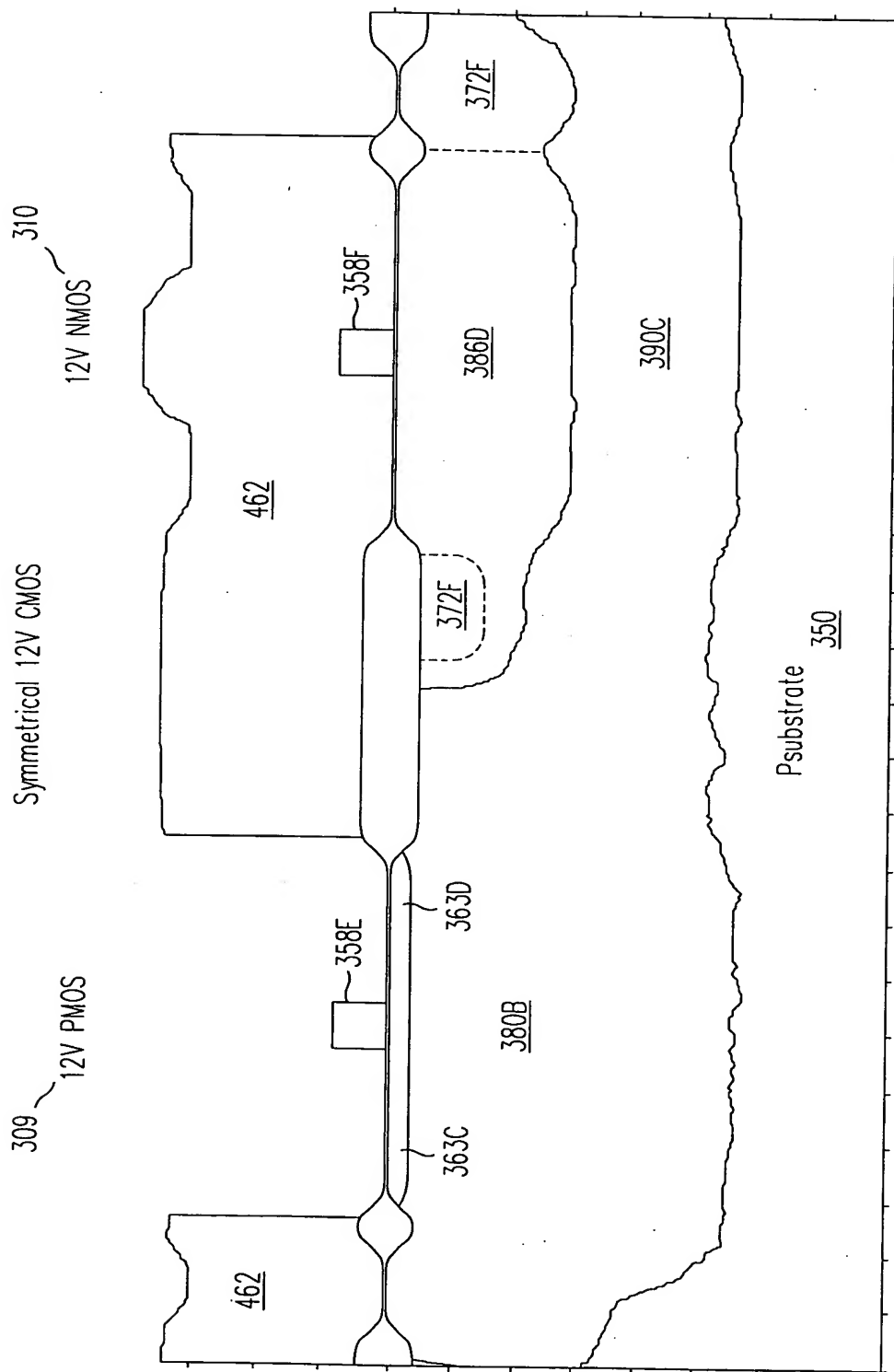
30V Lateral Trench DMOS ~ 308



P Body Mask and Implant-First Stage

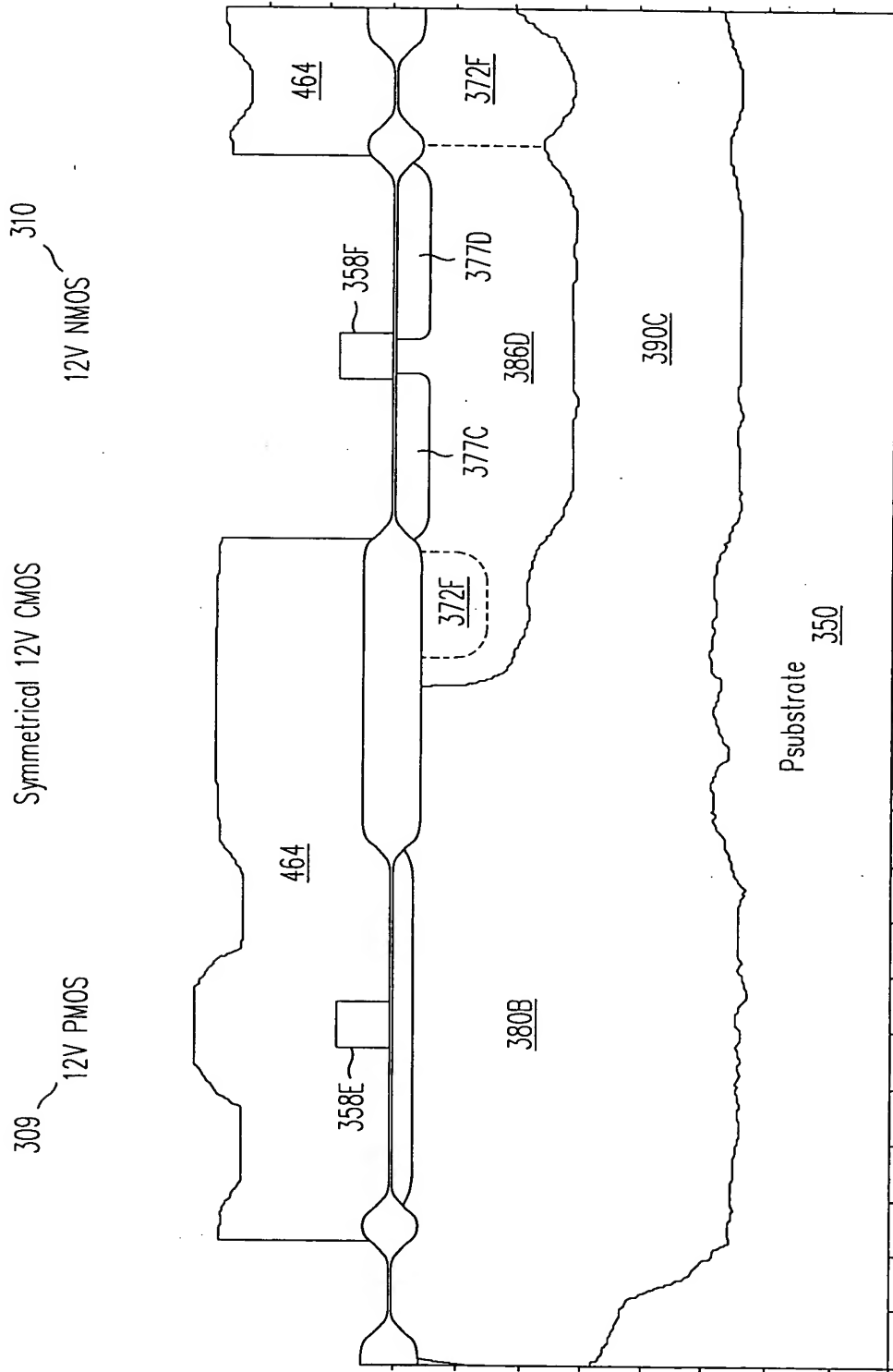
FIG. 55D





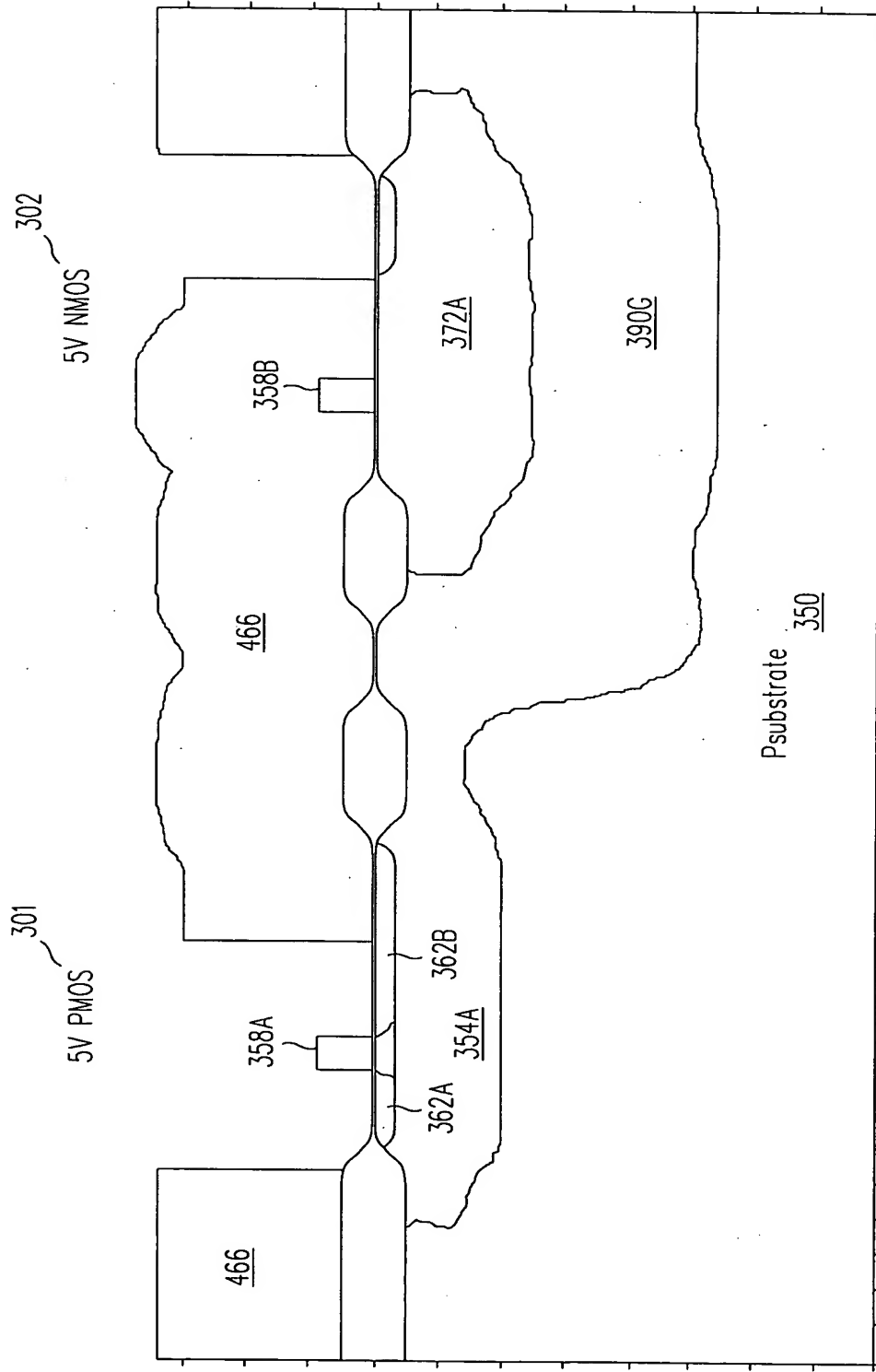
12V P-LDD Implant

FIG. 57E



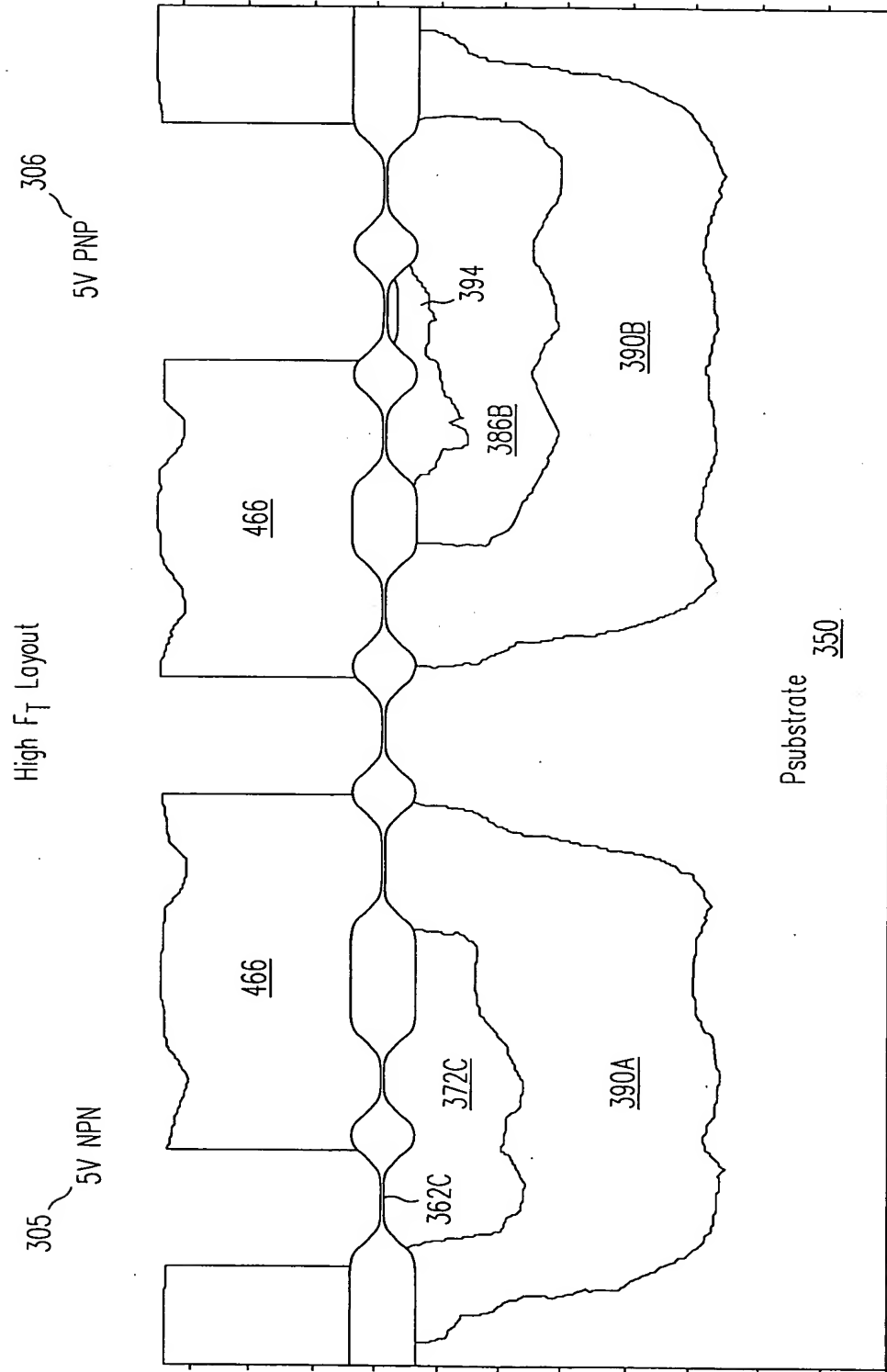
12V N-LDD Implant

**FIG. 58E**



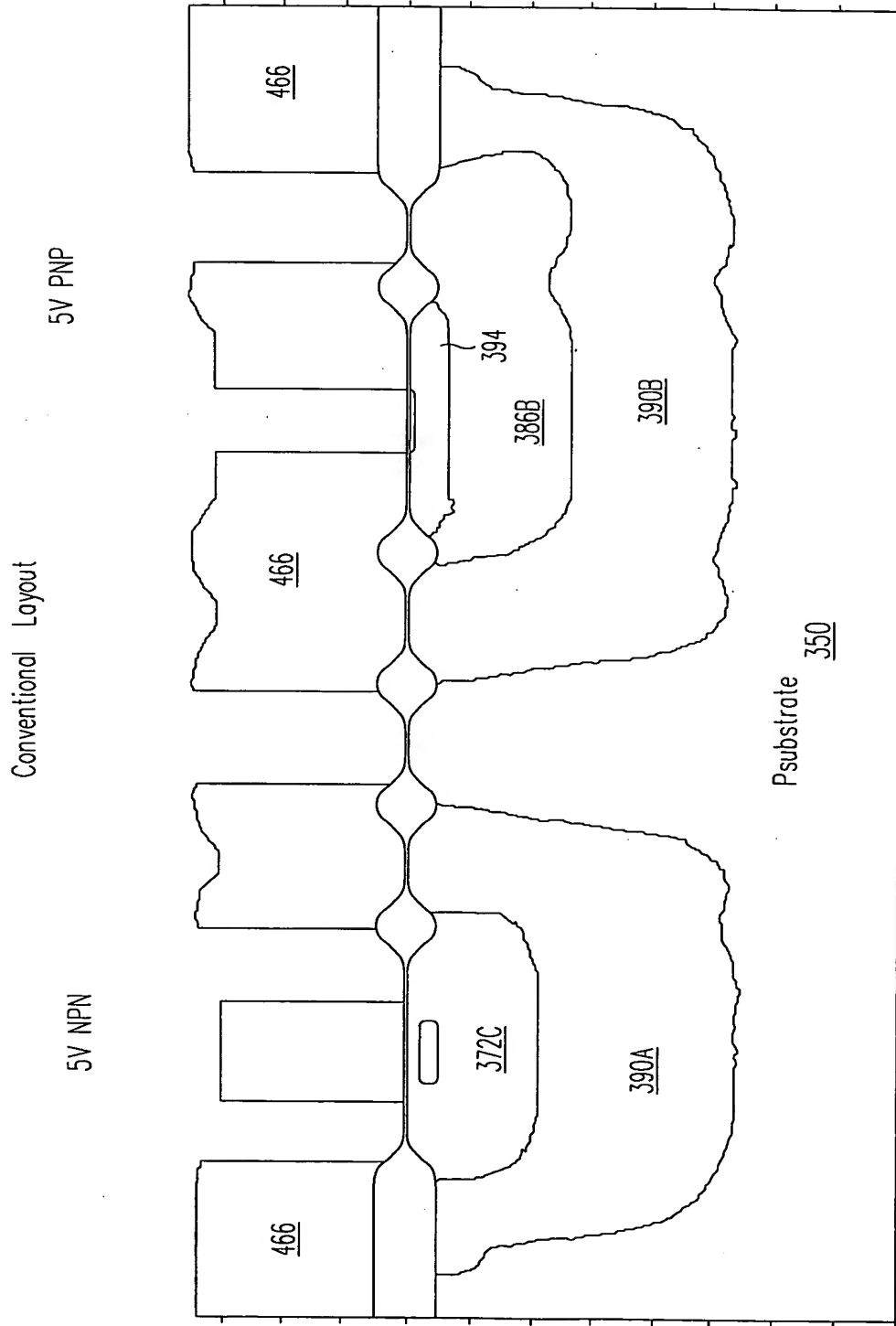
5V P-LDD Implant

FIG. 59A



5V P-LDD Implant

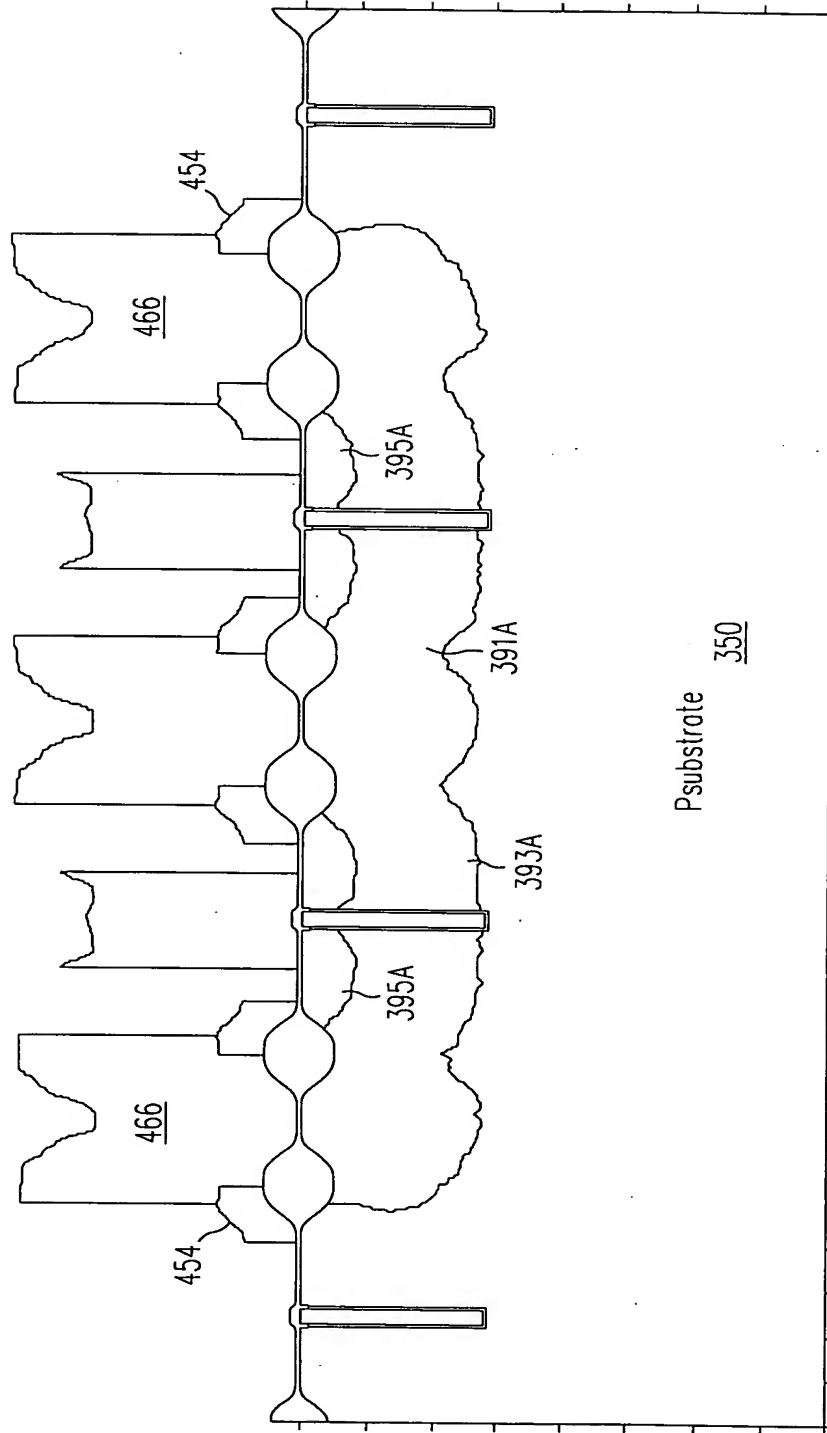
FIG. 59B



5V P-LDD Implant

FIG. 59C

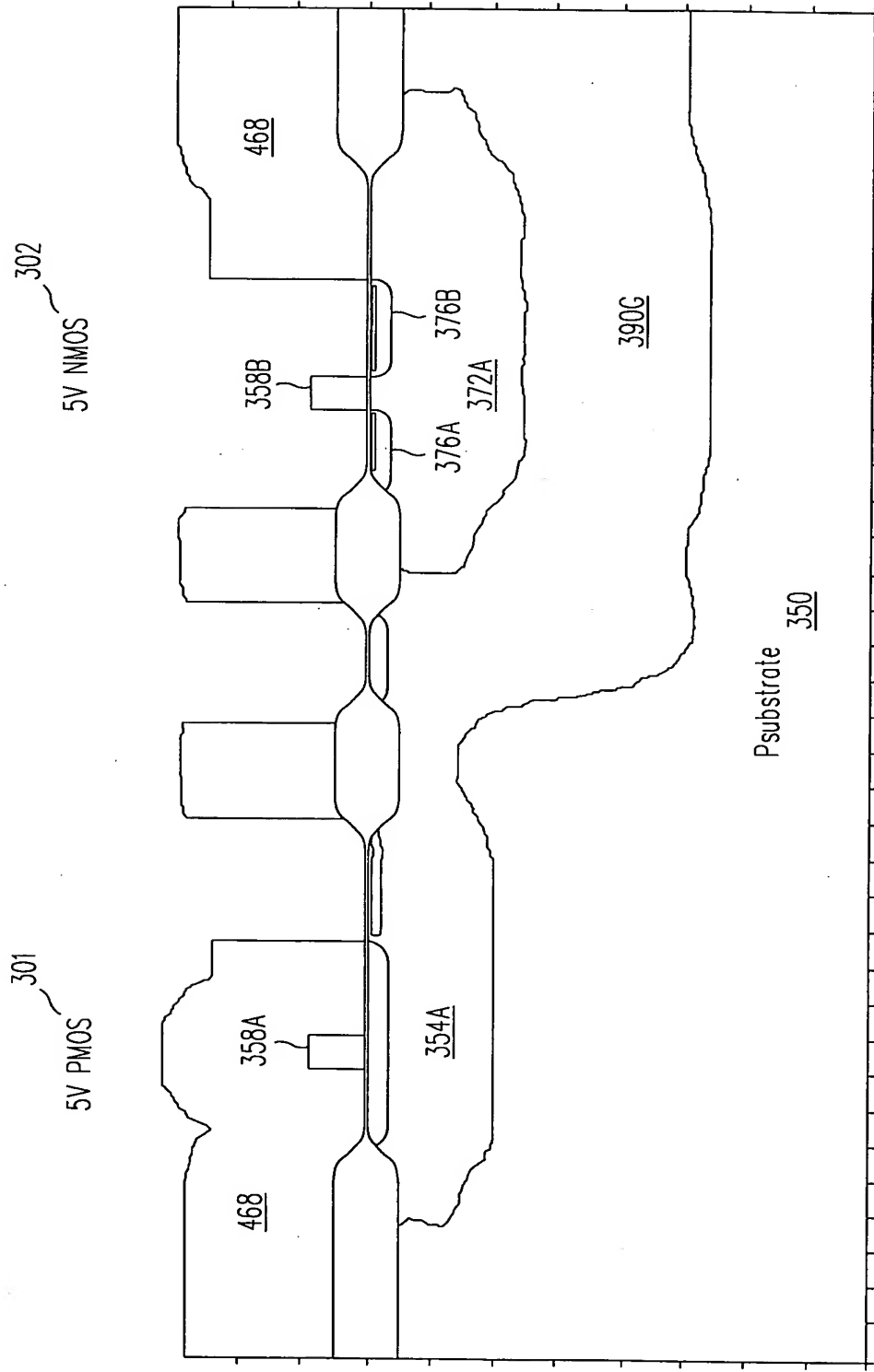
30V Lateral Trench DMOS ~ 308



5V P-LDD Implant

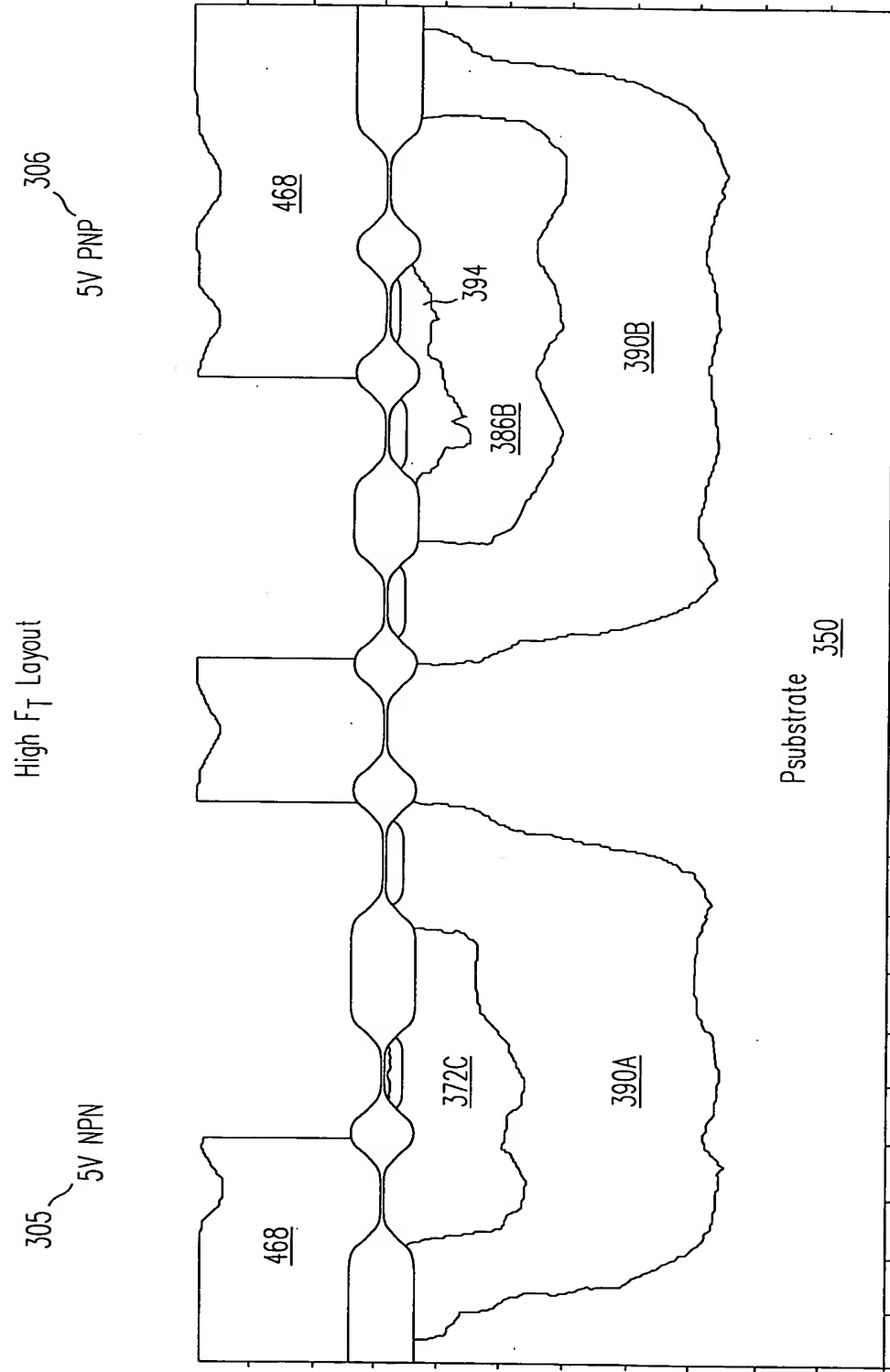
FIG. 59D





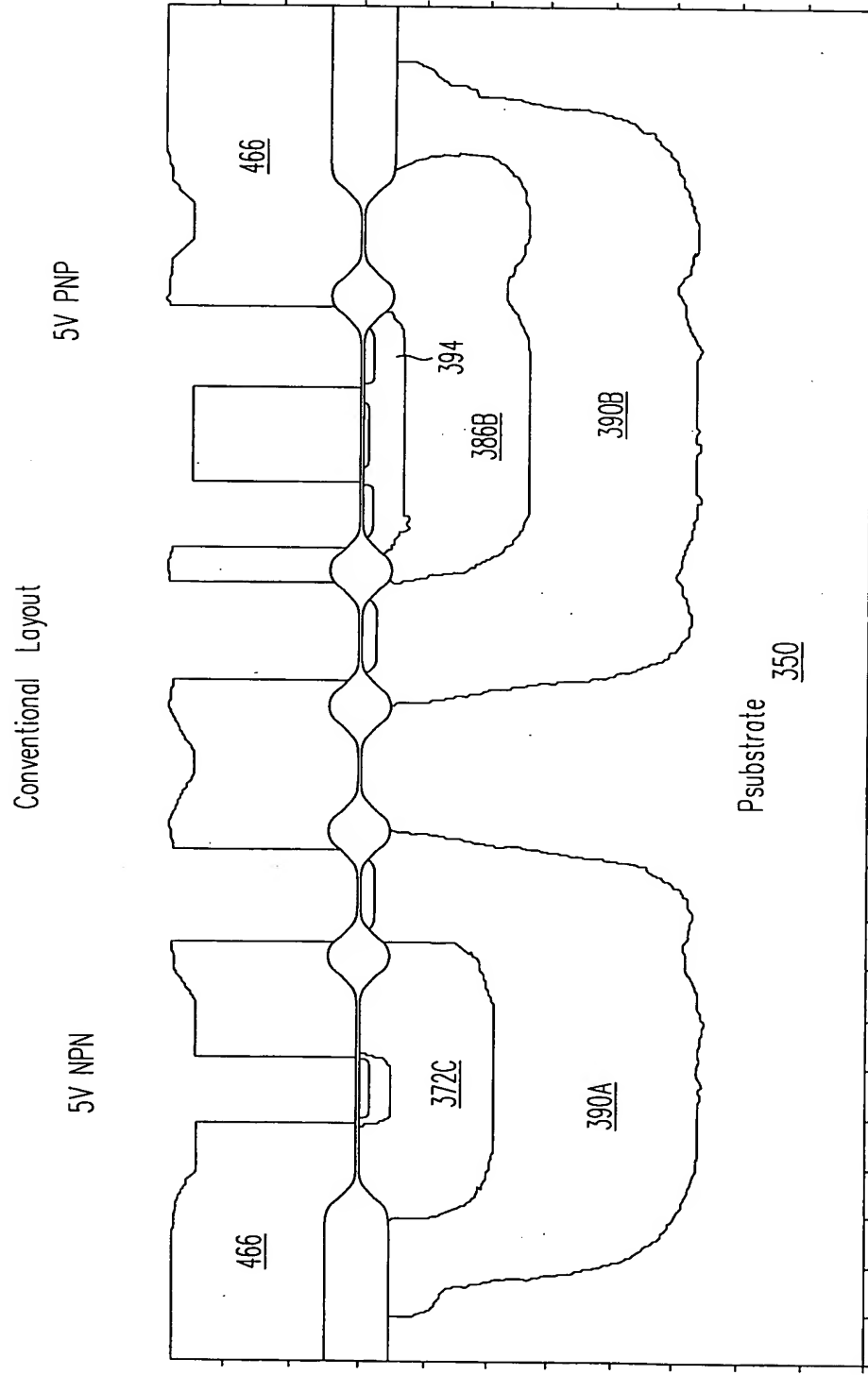
5V N-LDD Implant

**FIG. 60A**



5V N-LDD Implant

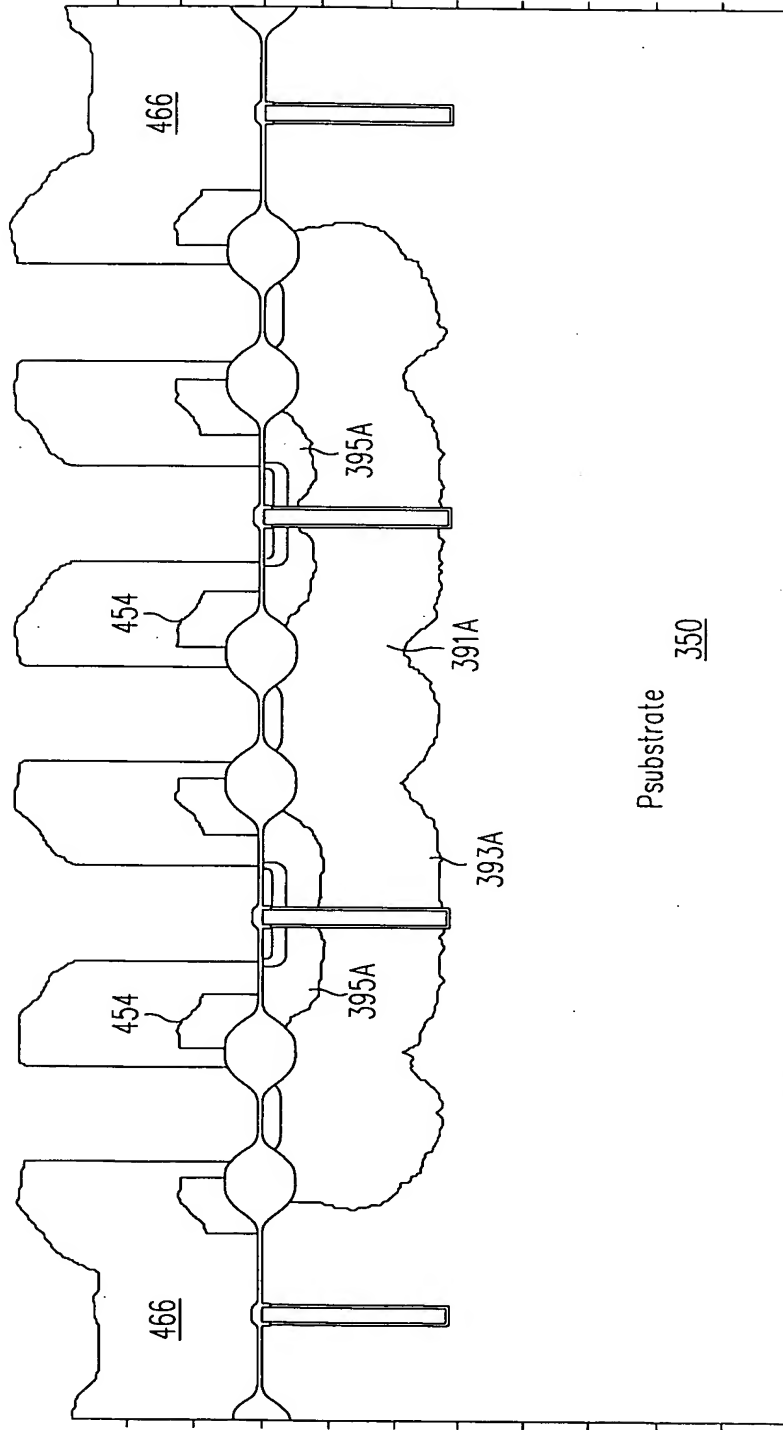
FIG. 60B



5V N-LDD Implant

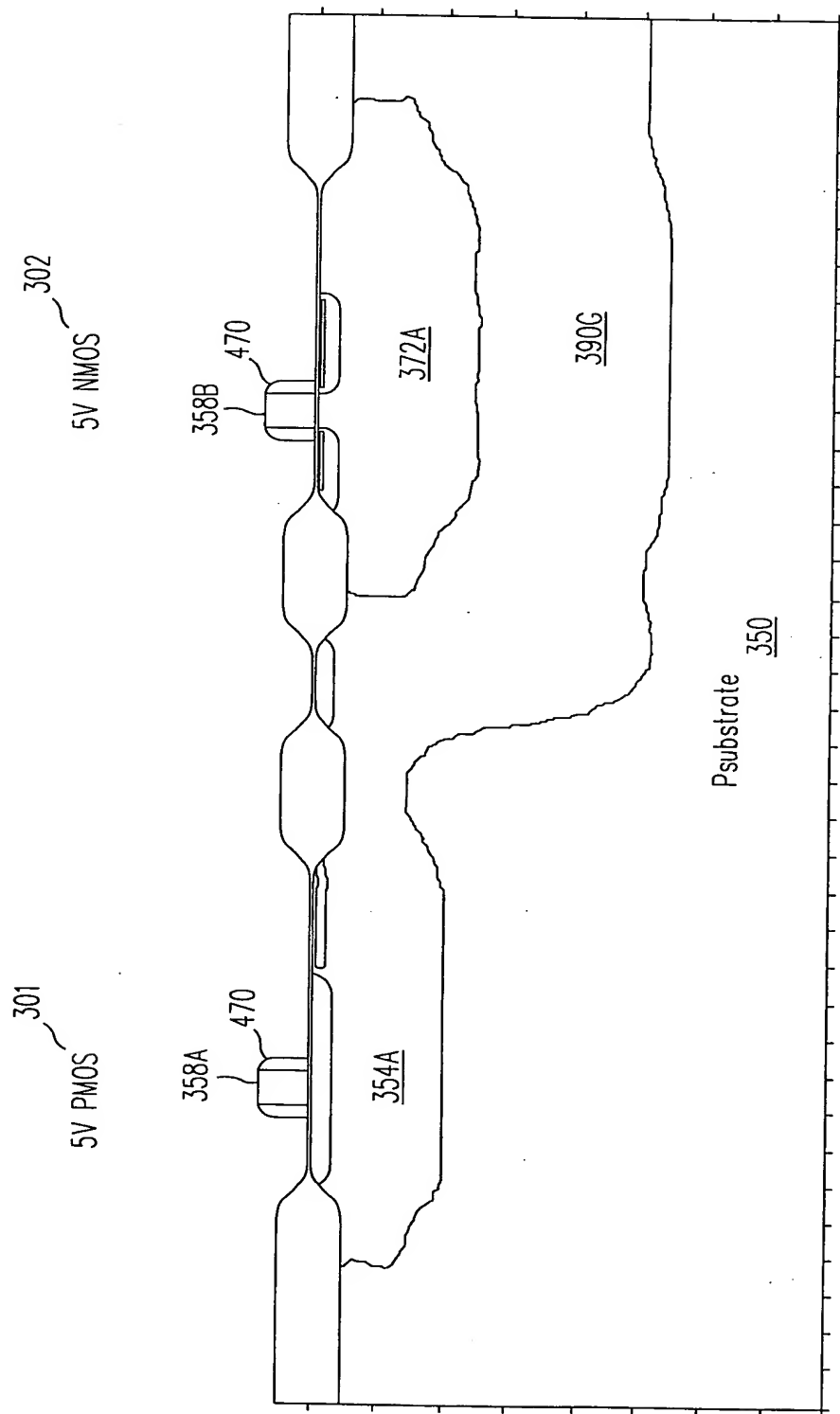
*FIG. 60C*

30V Lateral Trench DMOS ~ 308



5V N-LDD Implant

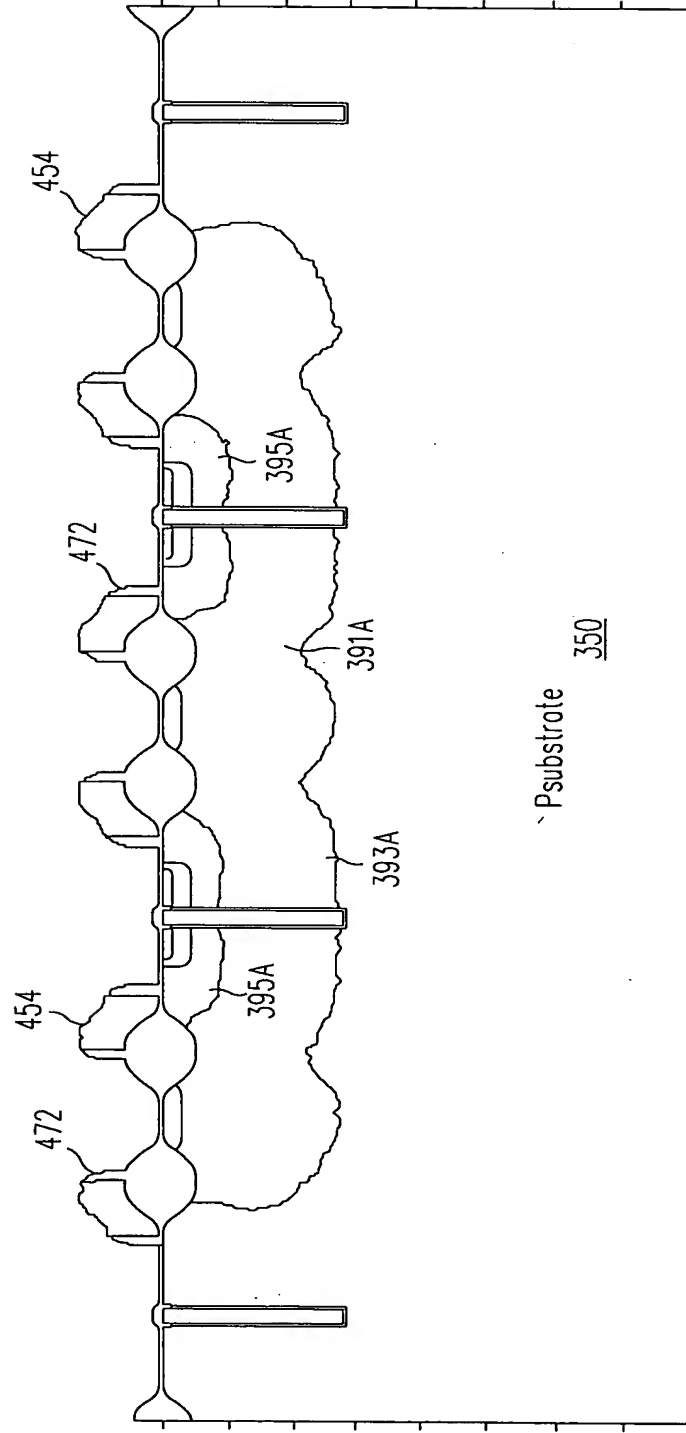
**FIG. 60D**



Sidewall Spacers

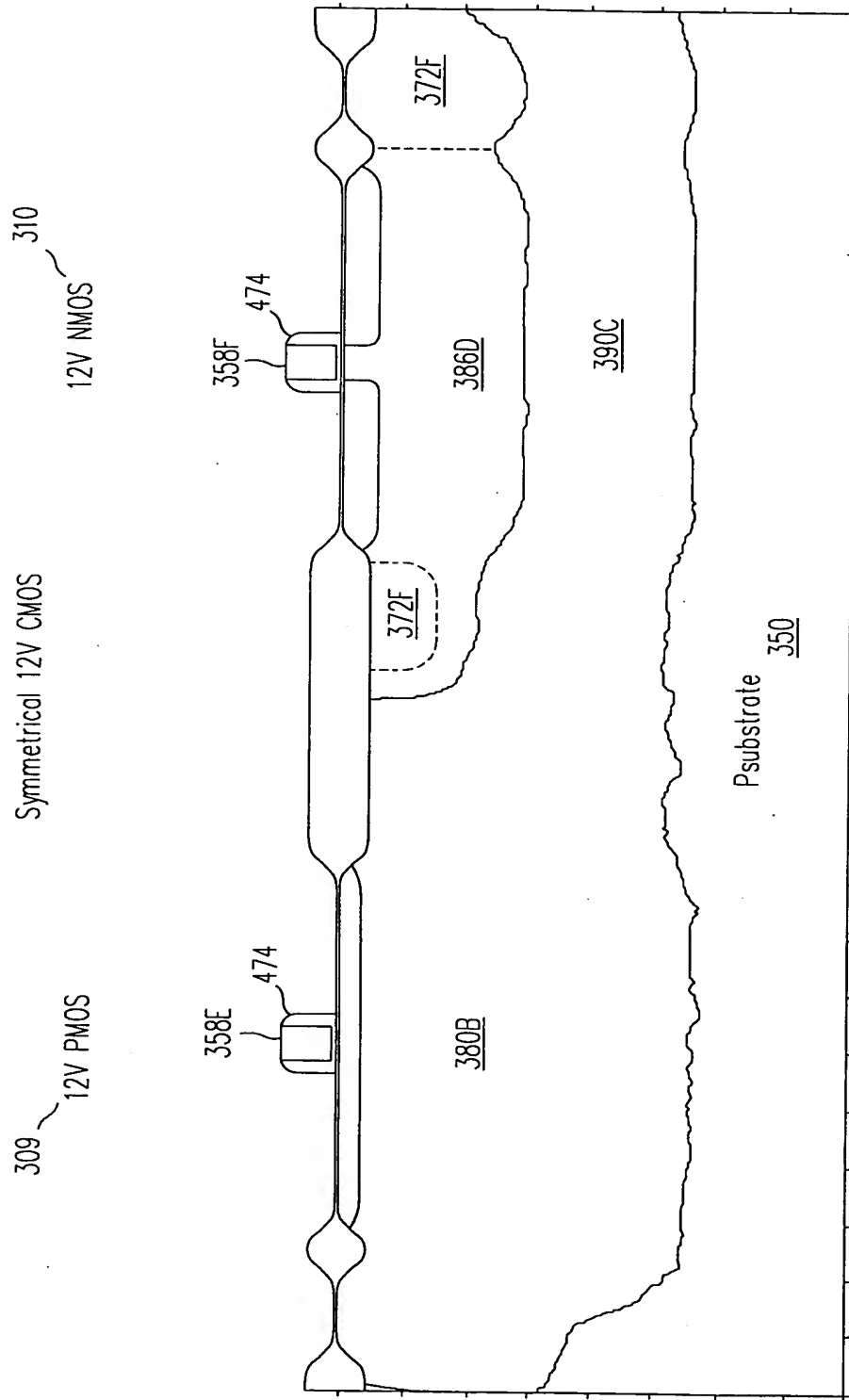
FIG. 61A

30V Lateral Trench DMOS ~ 308



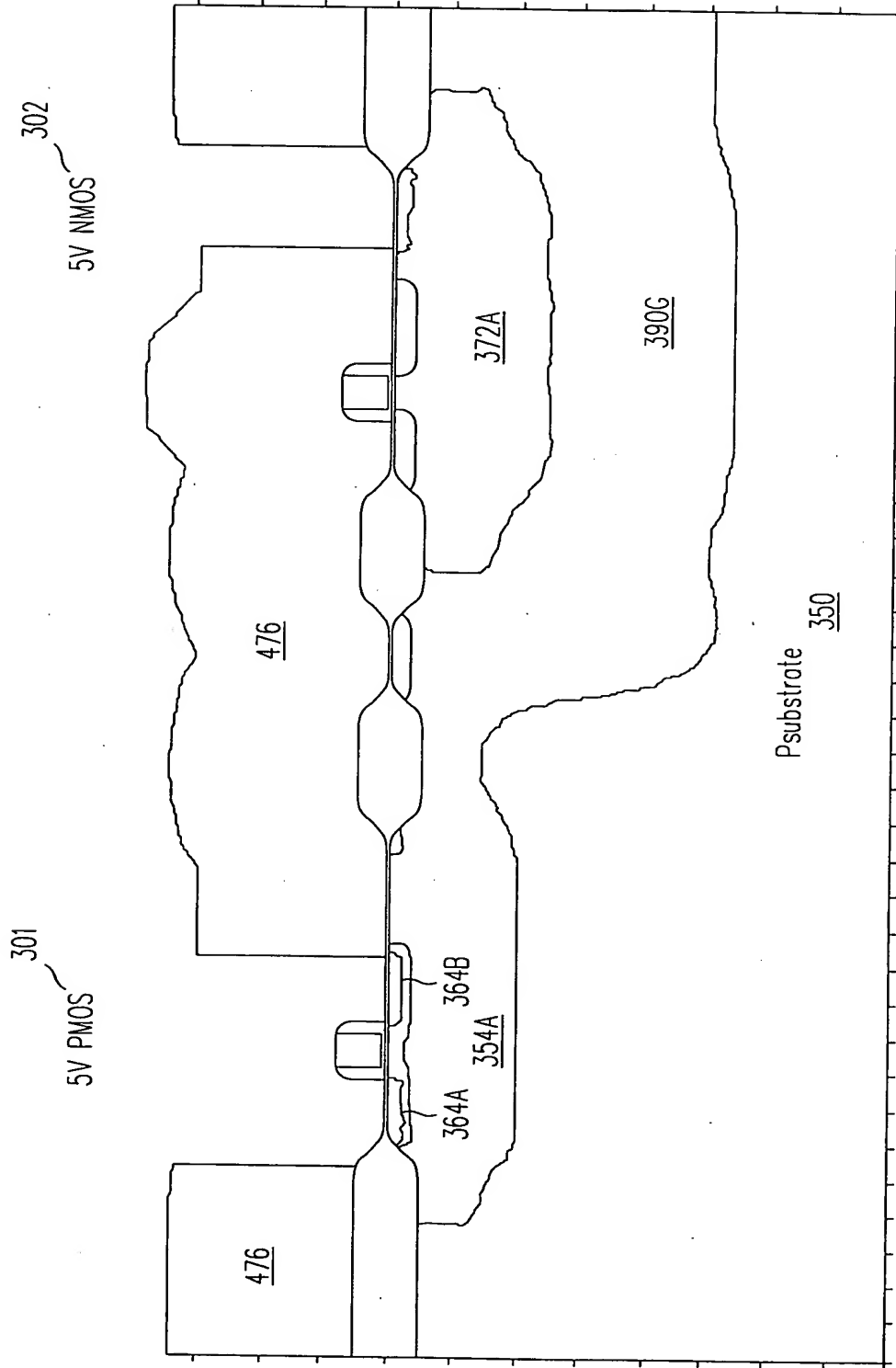
Sidewall Spacers

FIG. 61D



Sidewall Spacers

FIG. 61E



P+ Implant  
**FIG. 62A**



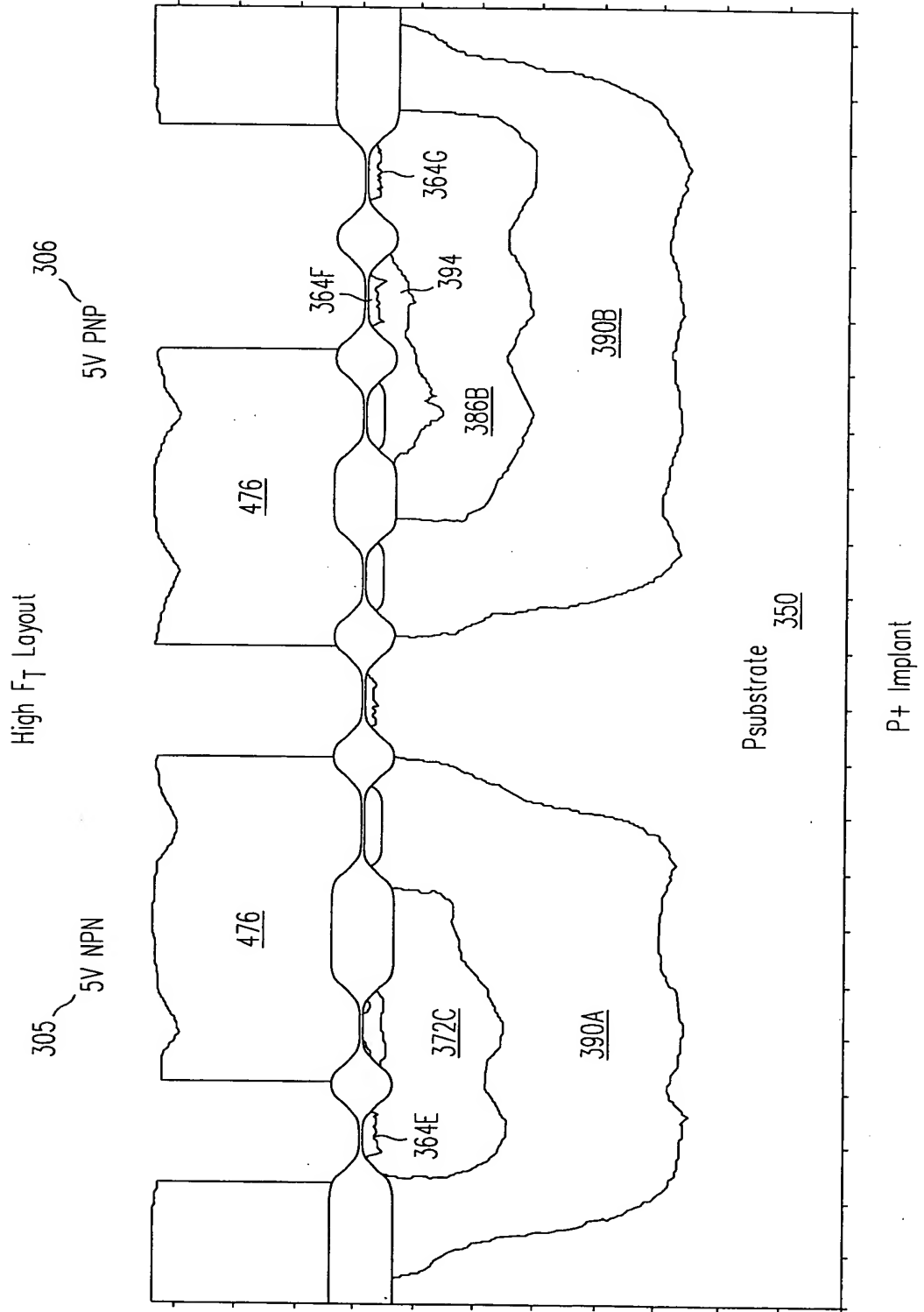
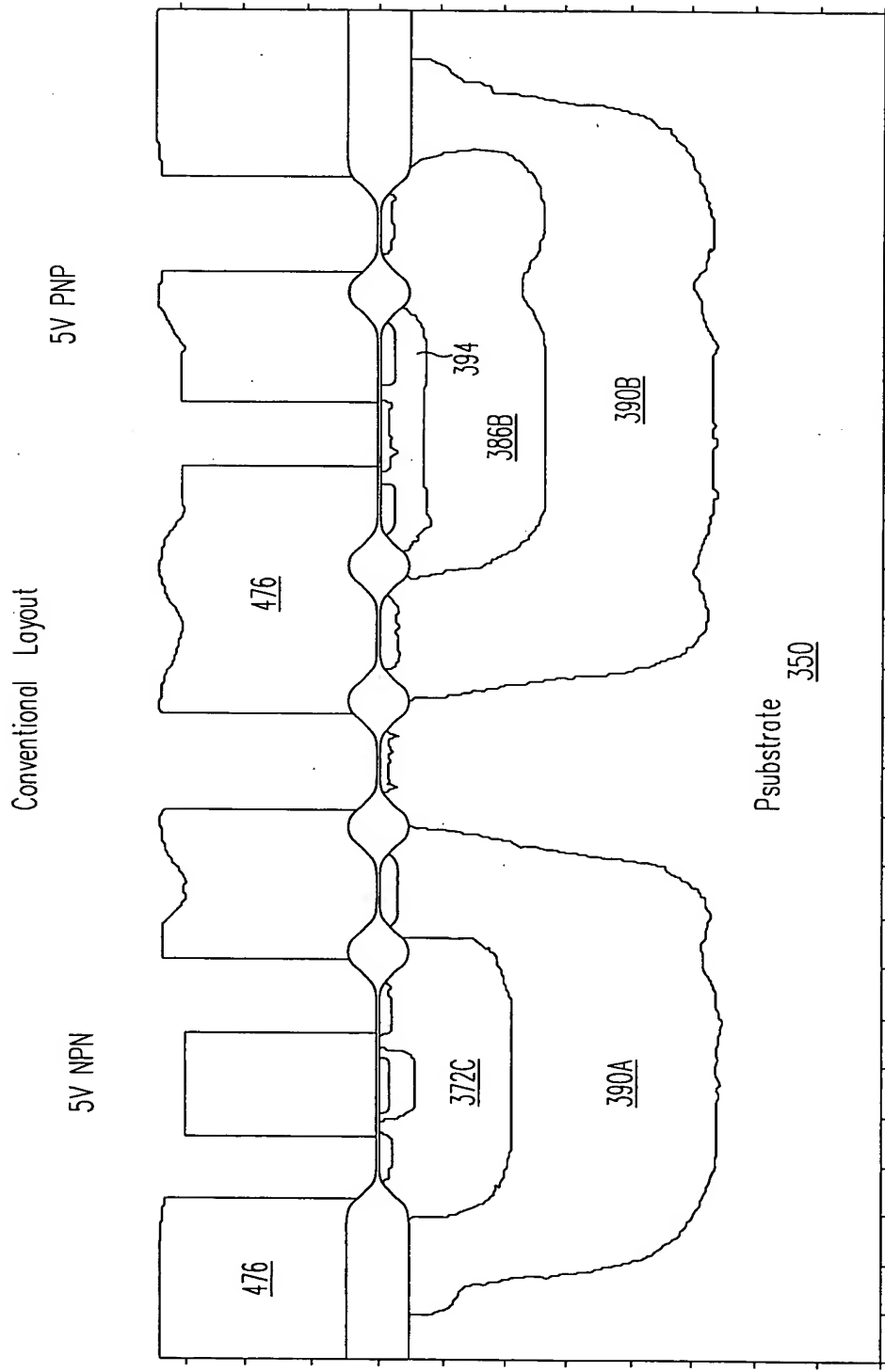


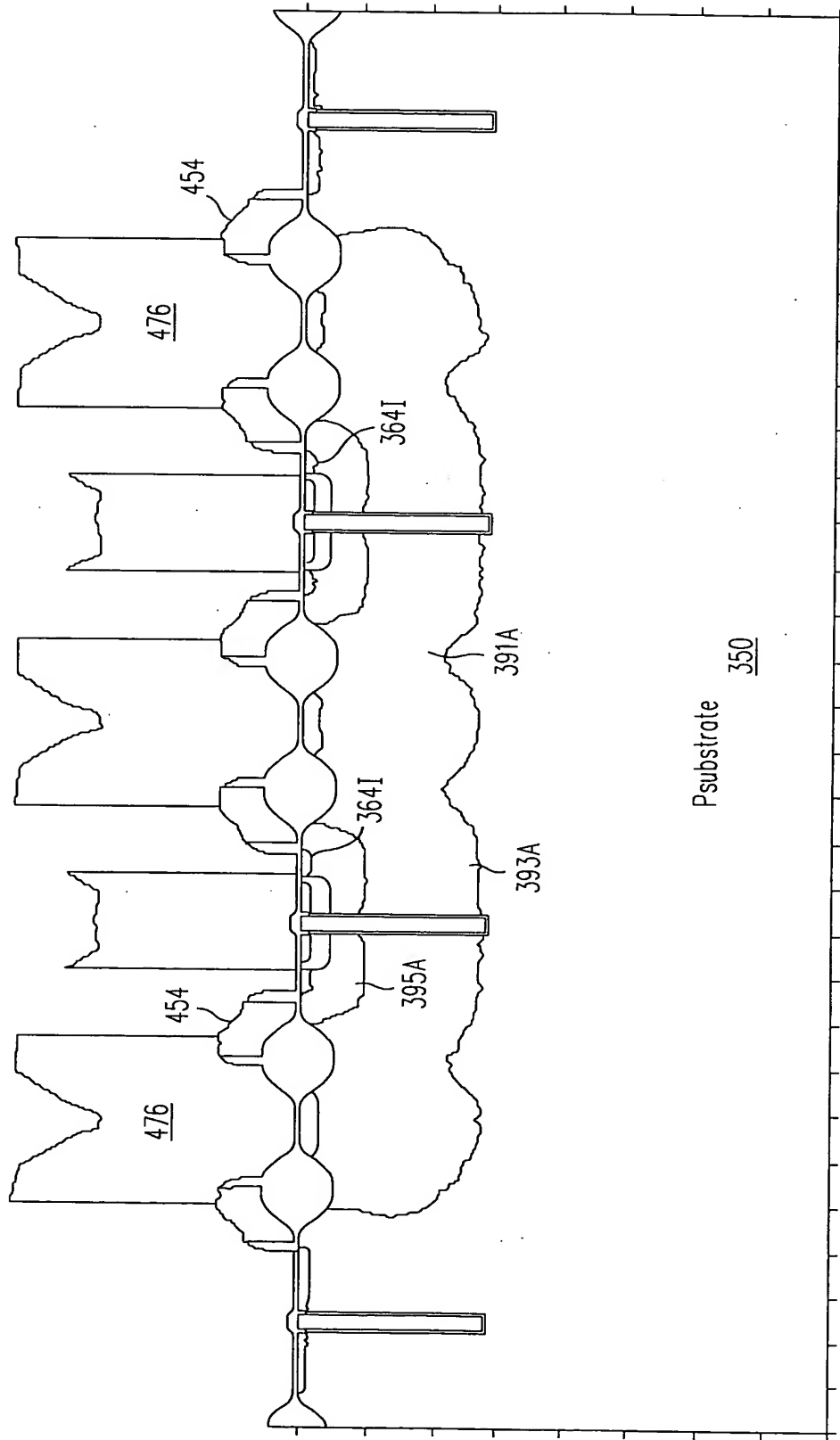
FIG. 62B

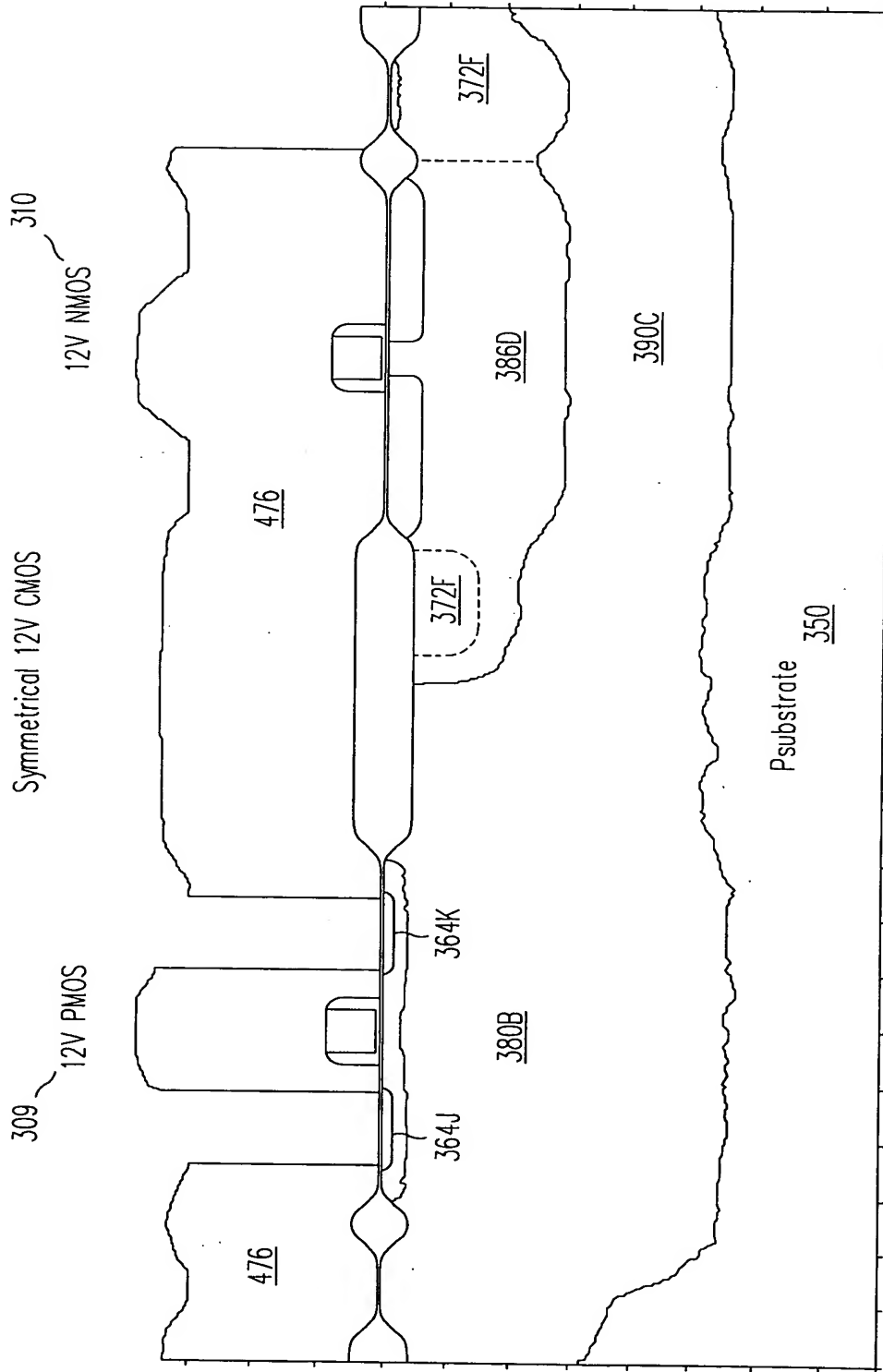


P+ Implant

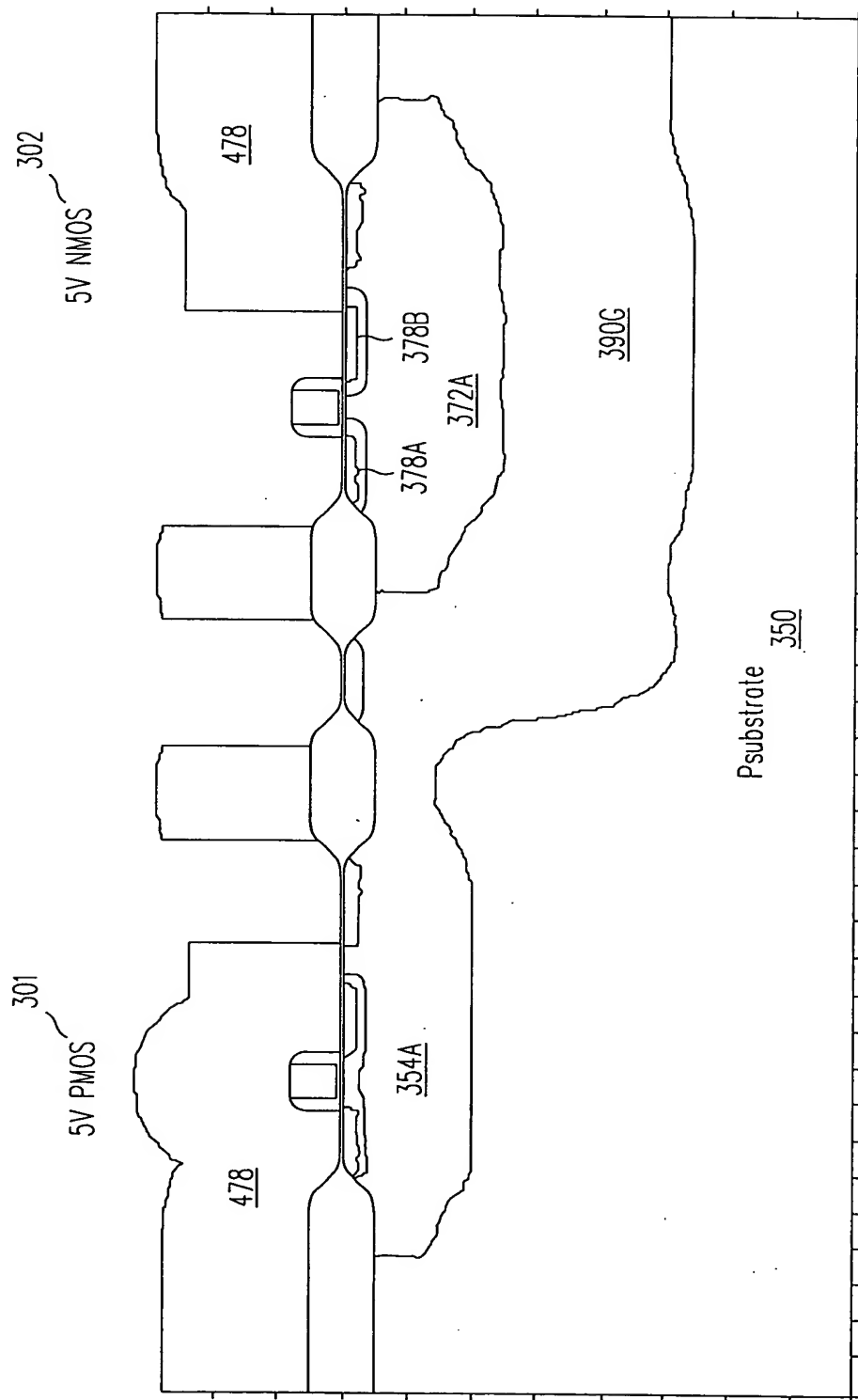
FIG. 62C

30V Lateral Trench DMOS ~ 308





**FIG. 62E**



N+ Implant  
FIG. 63A

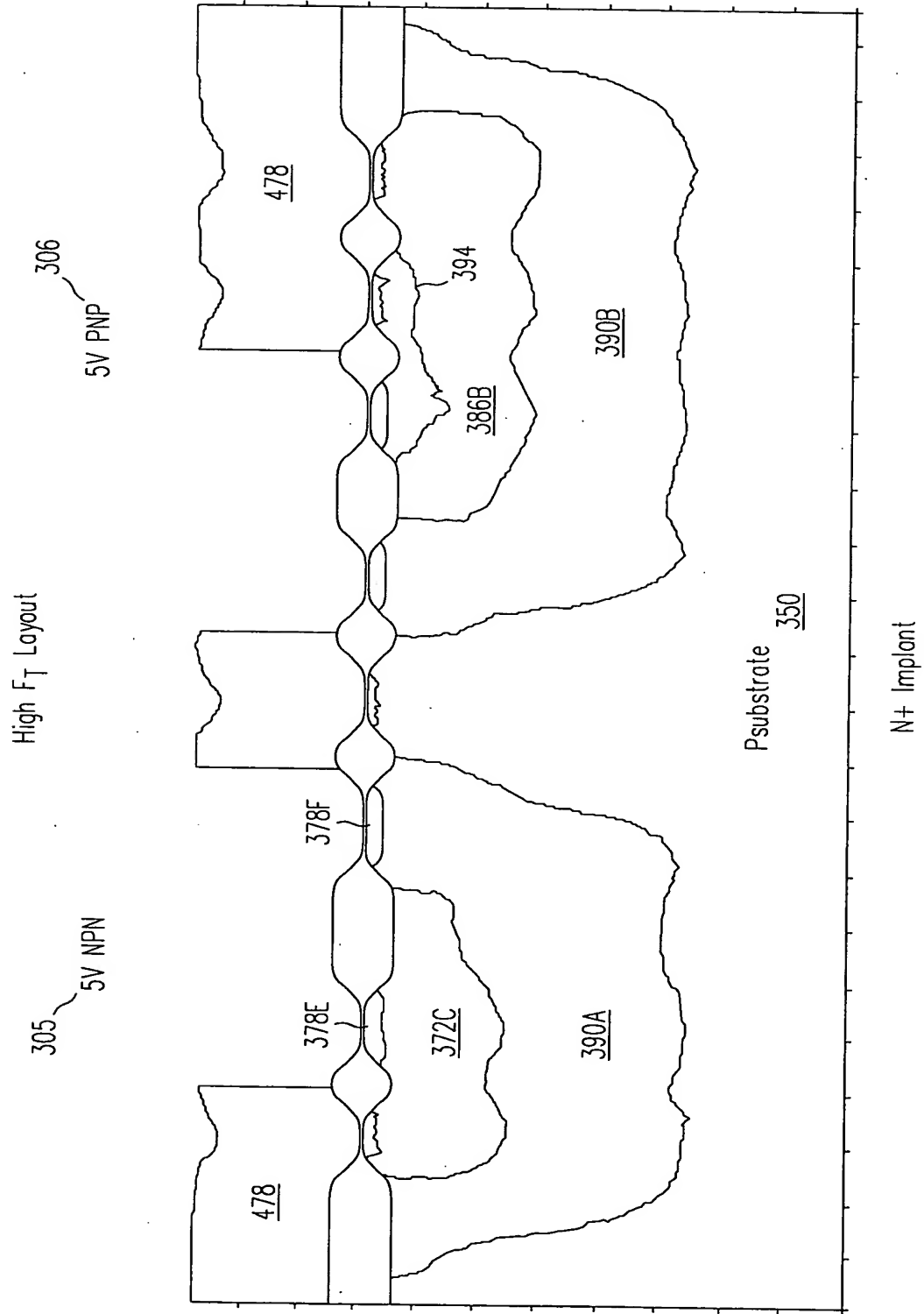
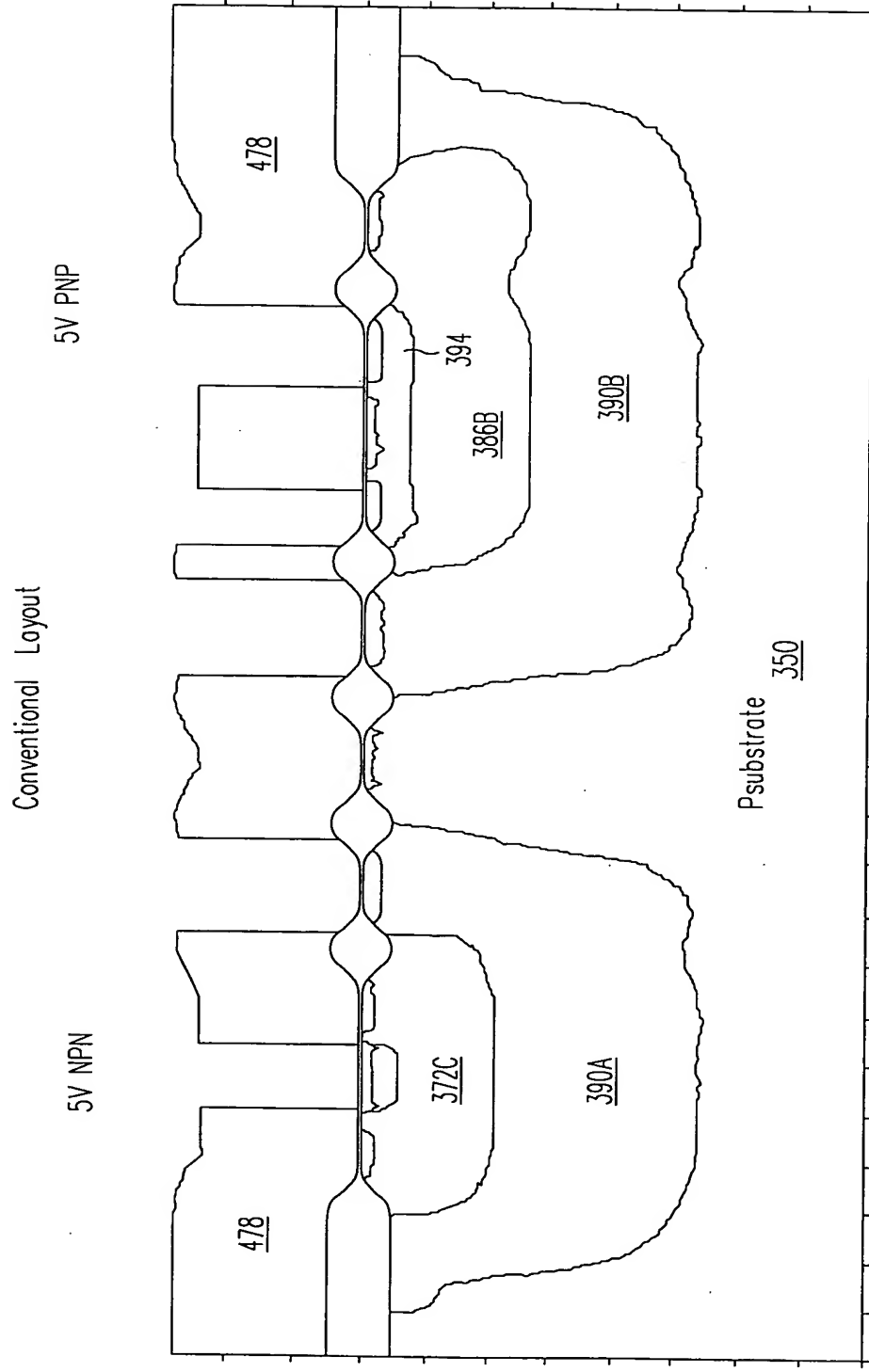


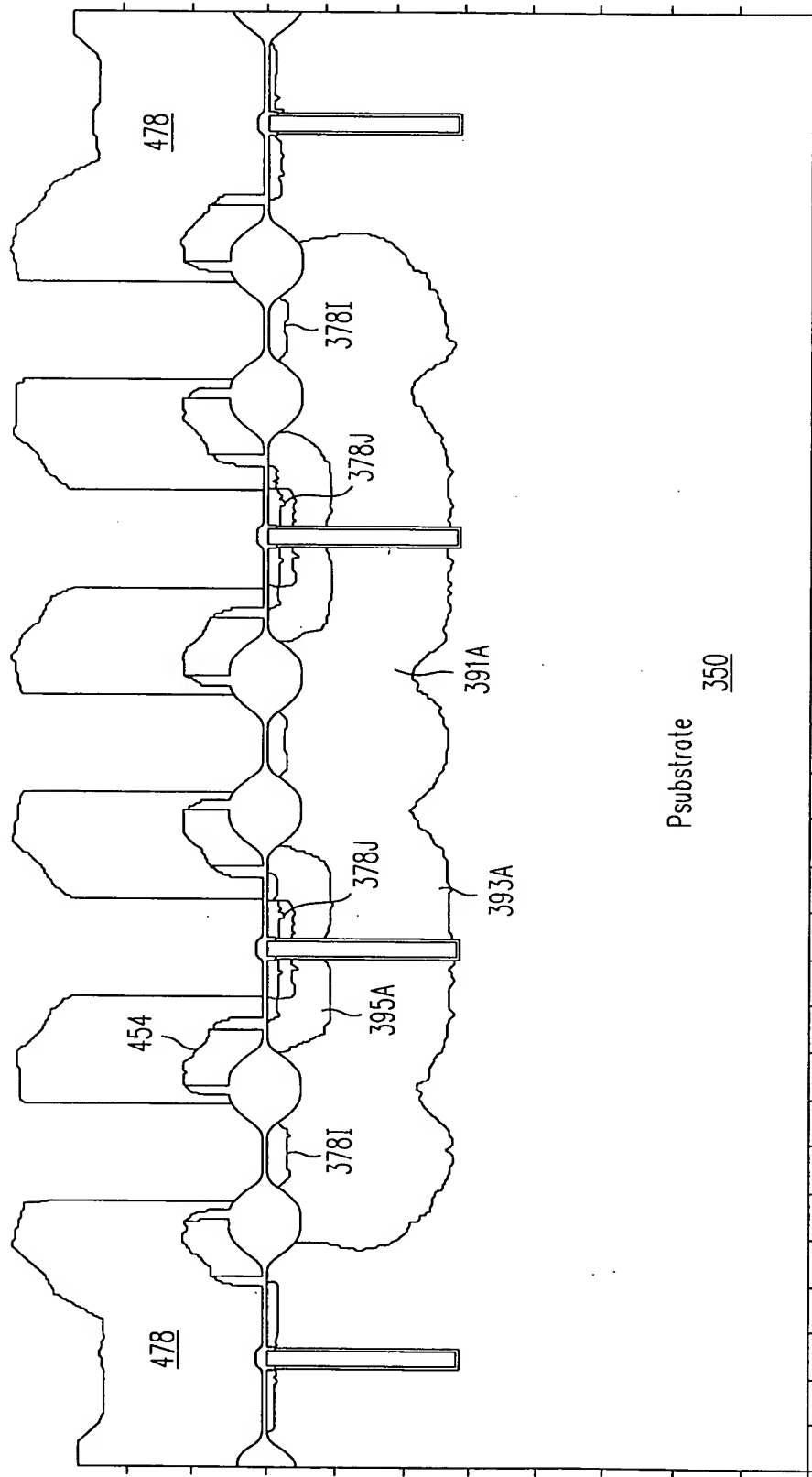
FIG. 63B



N+ Implant

*FIG. 63C*

30V Lateral Trench DMOS ~ 308

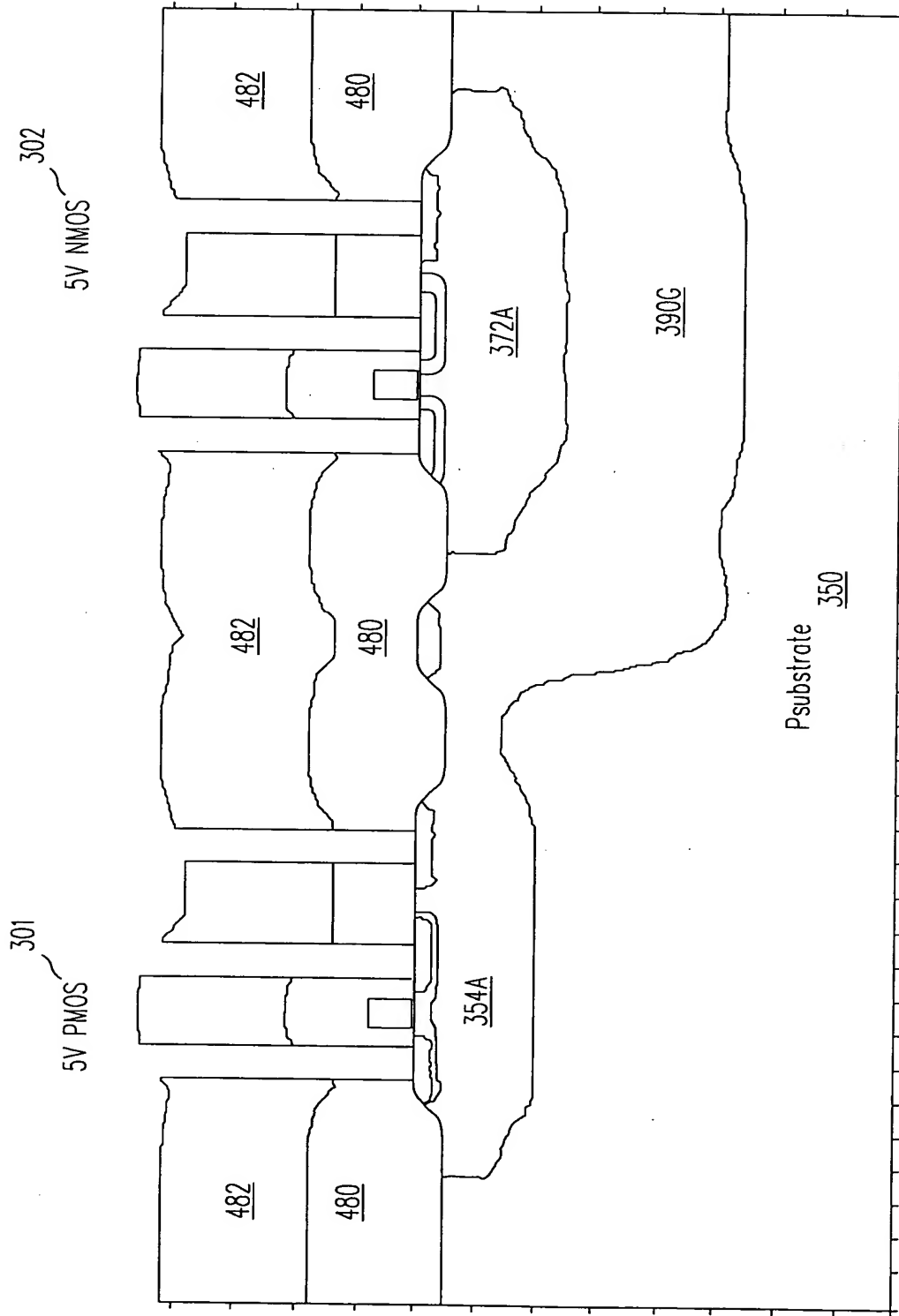


N+ Implant

FIG. 63D

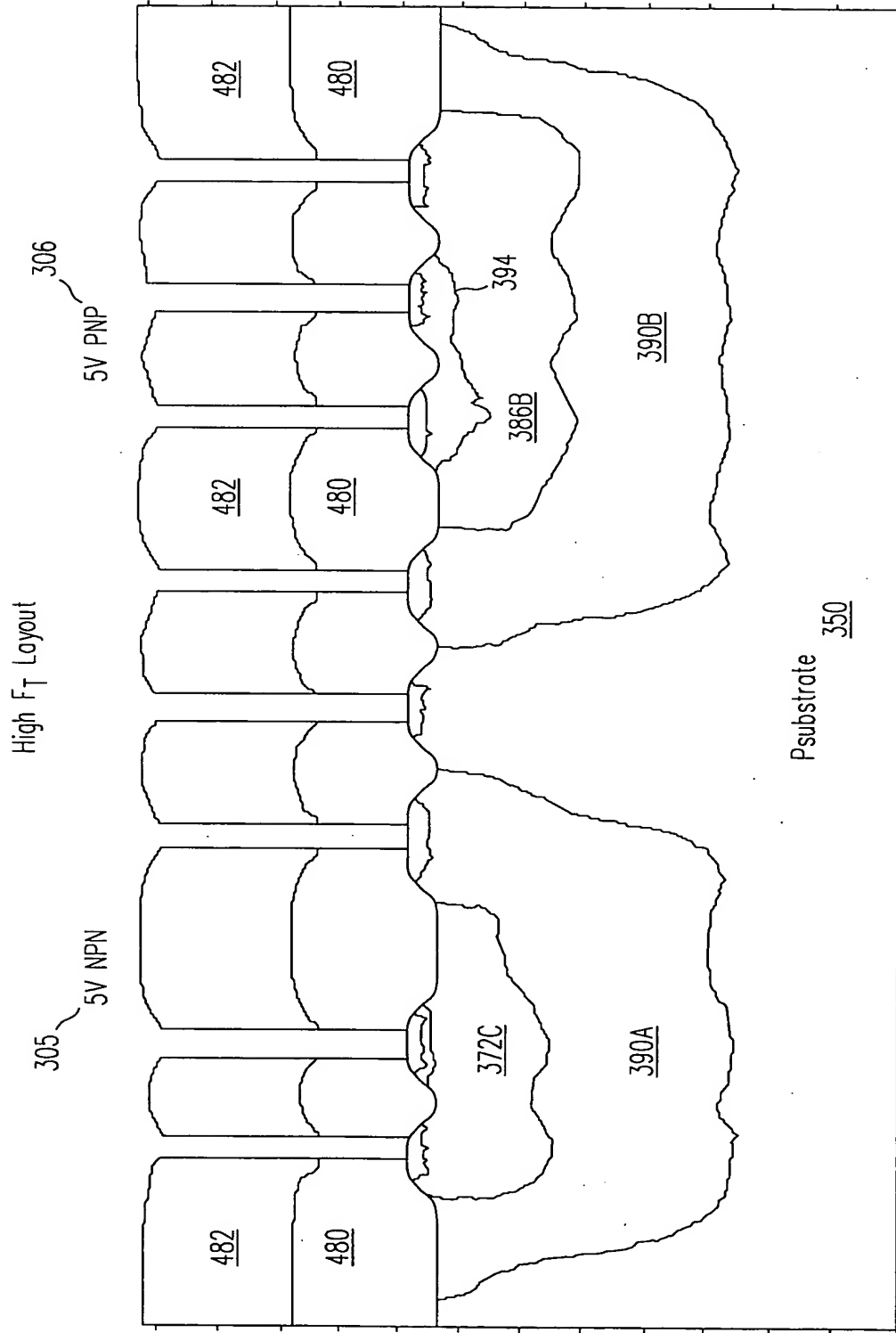


FIG. 63E



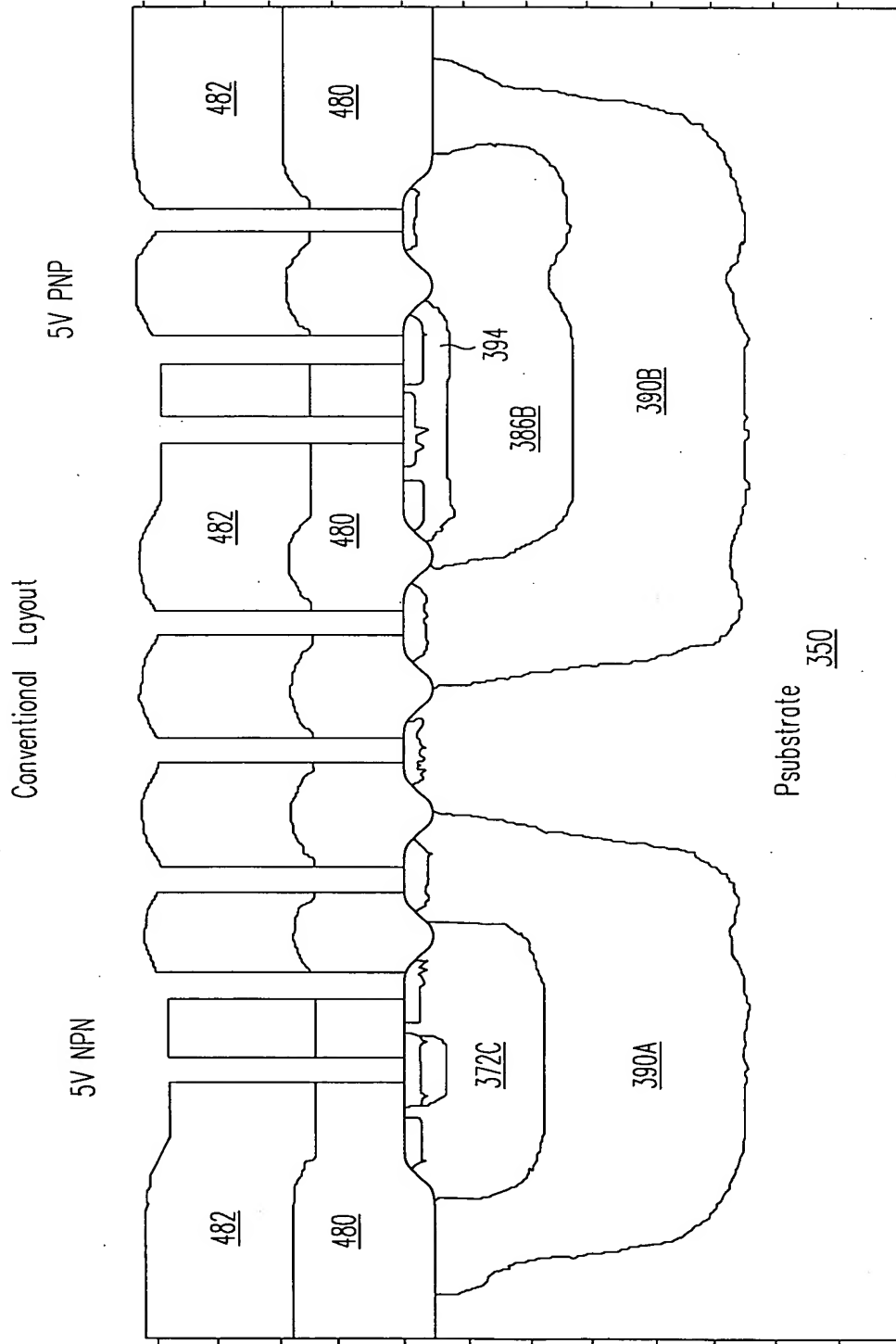
Interlayer Dielectric Deposition and Etch

**FIG. 64A**



Interlayer Dielectric Deposition and Etch

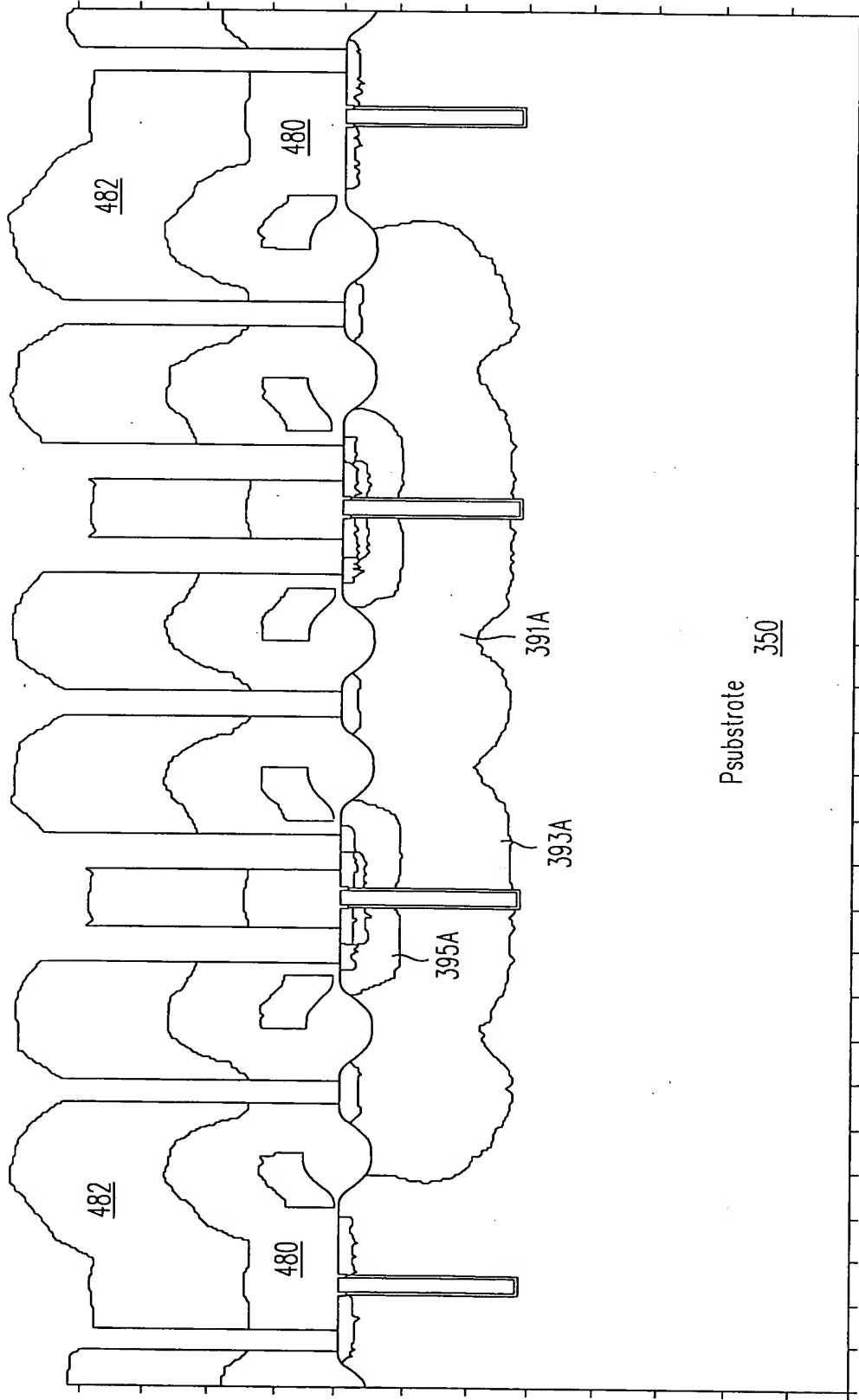
**FIG. 64B**



Interlayer Dielectric Deposition and Etch

FIG. 64C

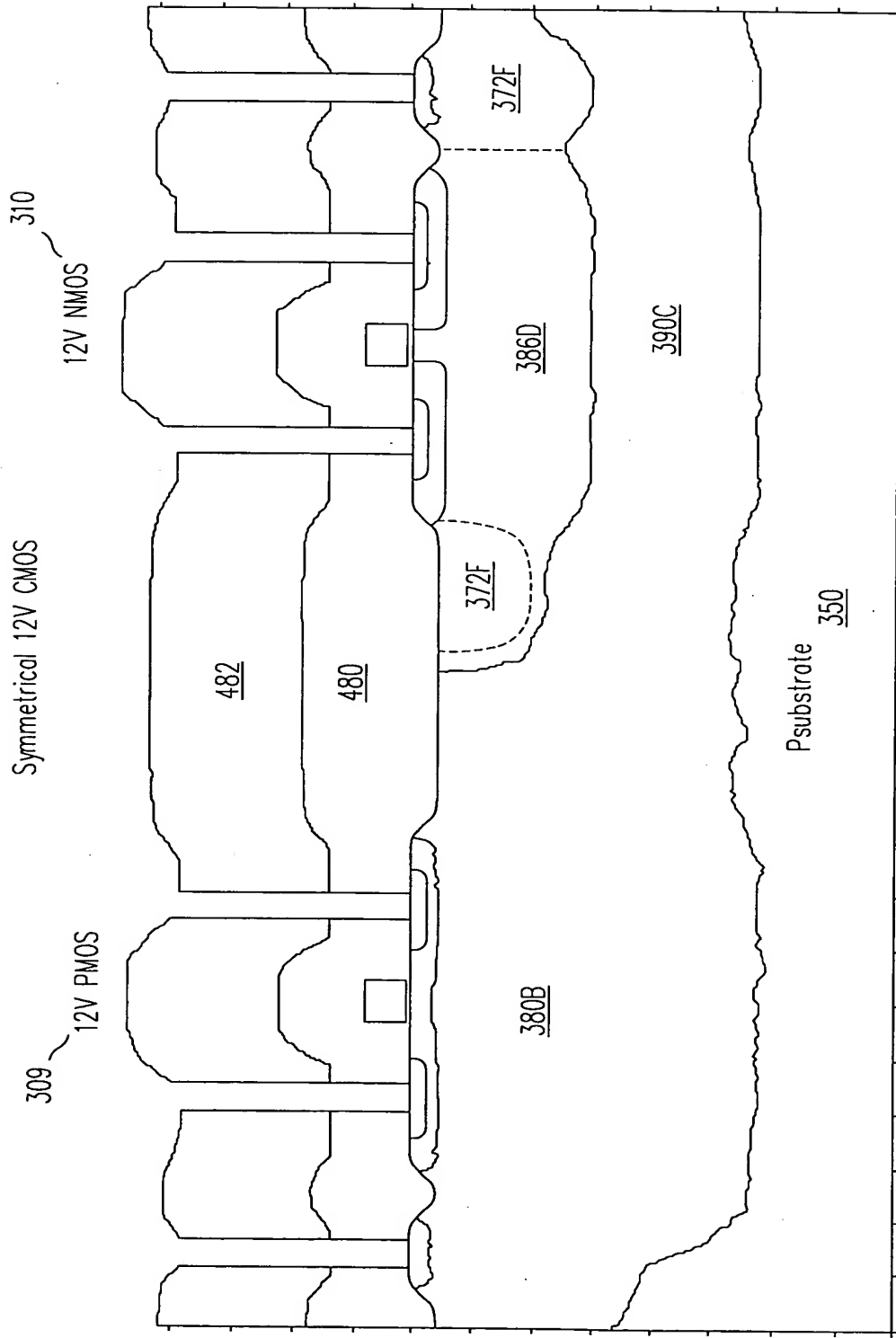
30V Lateral Trench DMOS ~ 308



Psubstrate 350

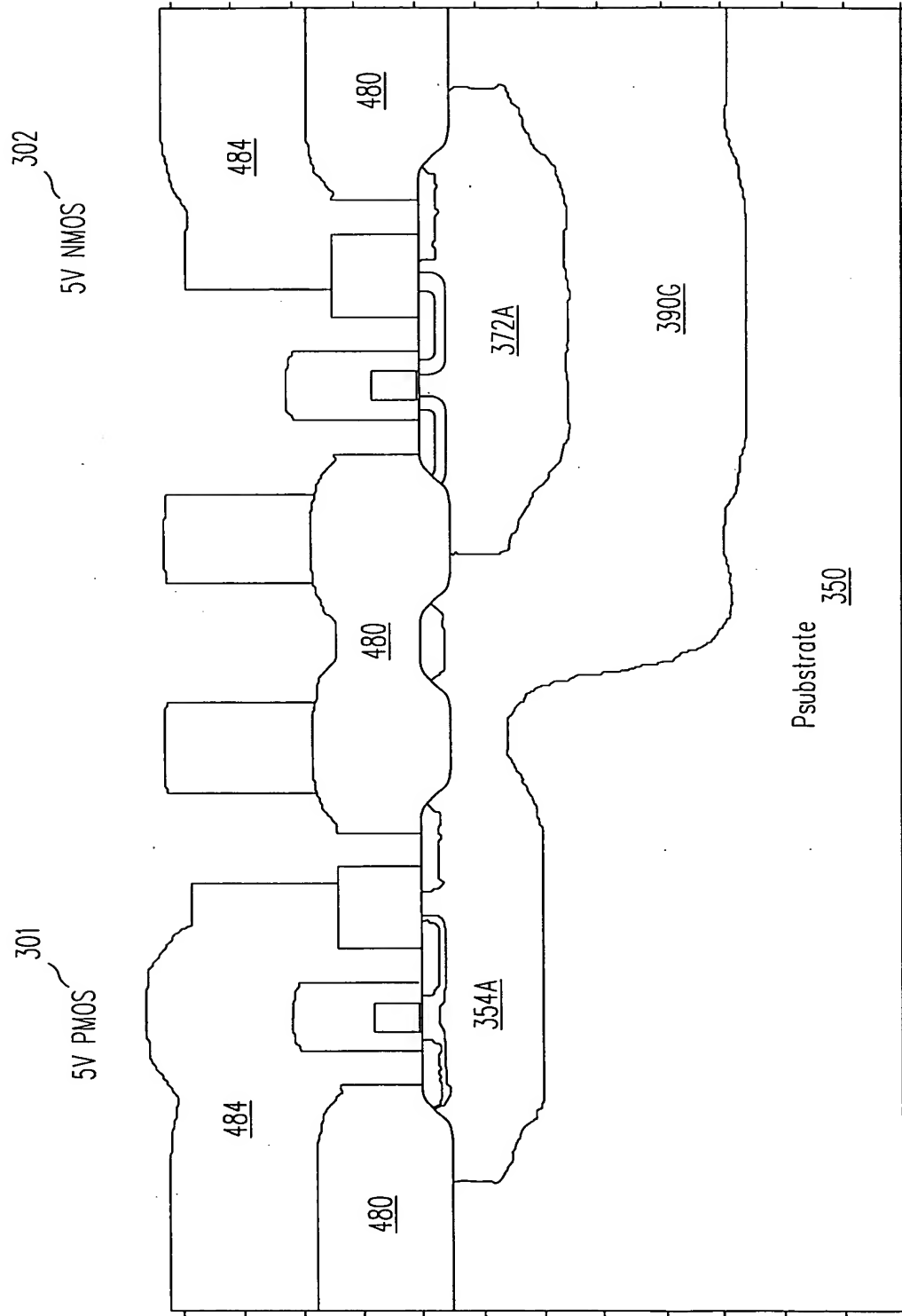
Interlayer Dielectric Deposition and Etch

FIG. 64D



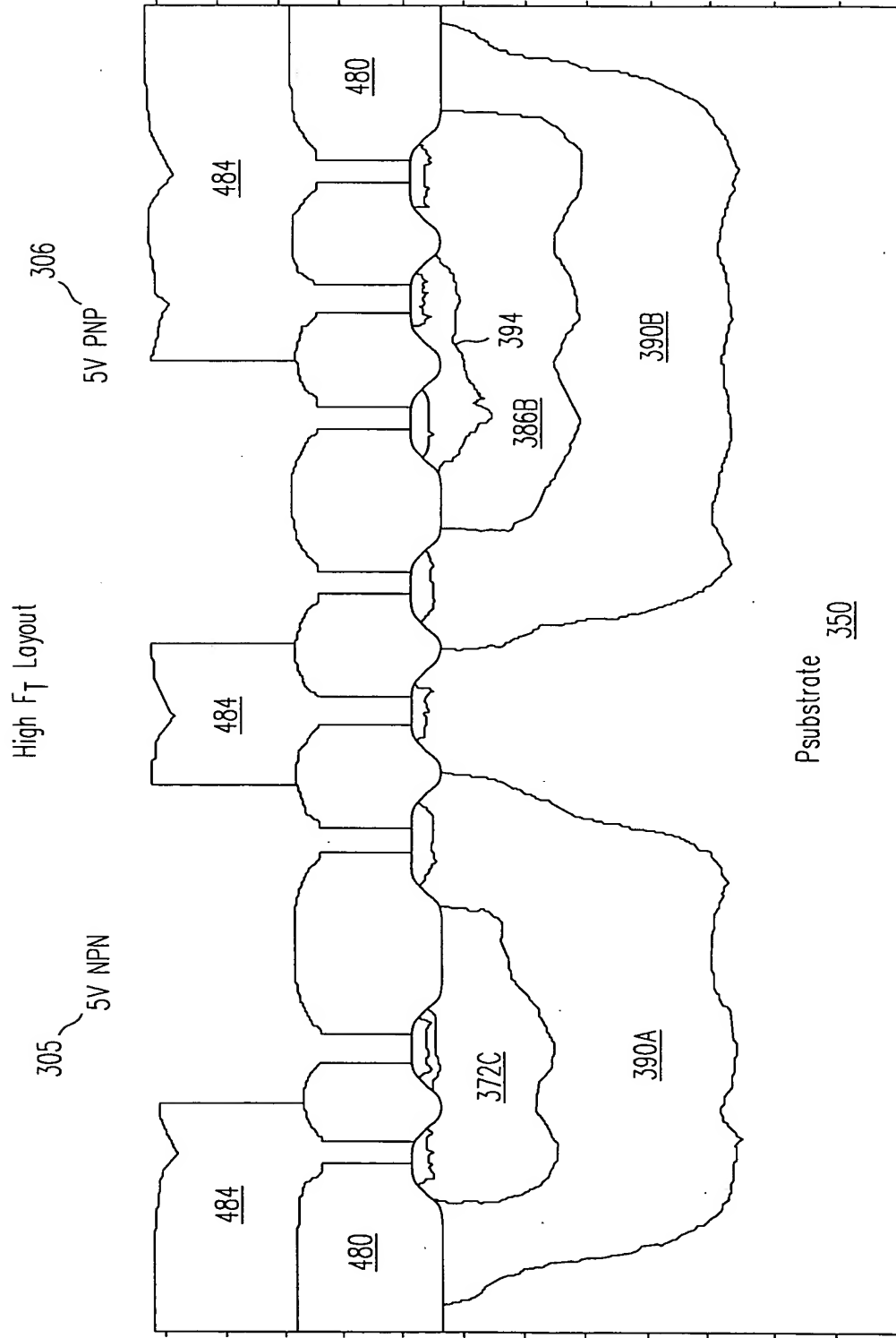
Interlayer Dielectric Deposition and Etch

FIG. 64E



N-plug Mask and Implant

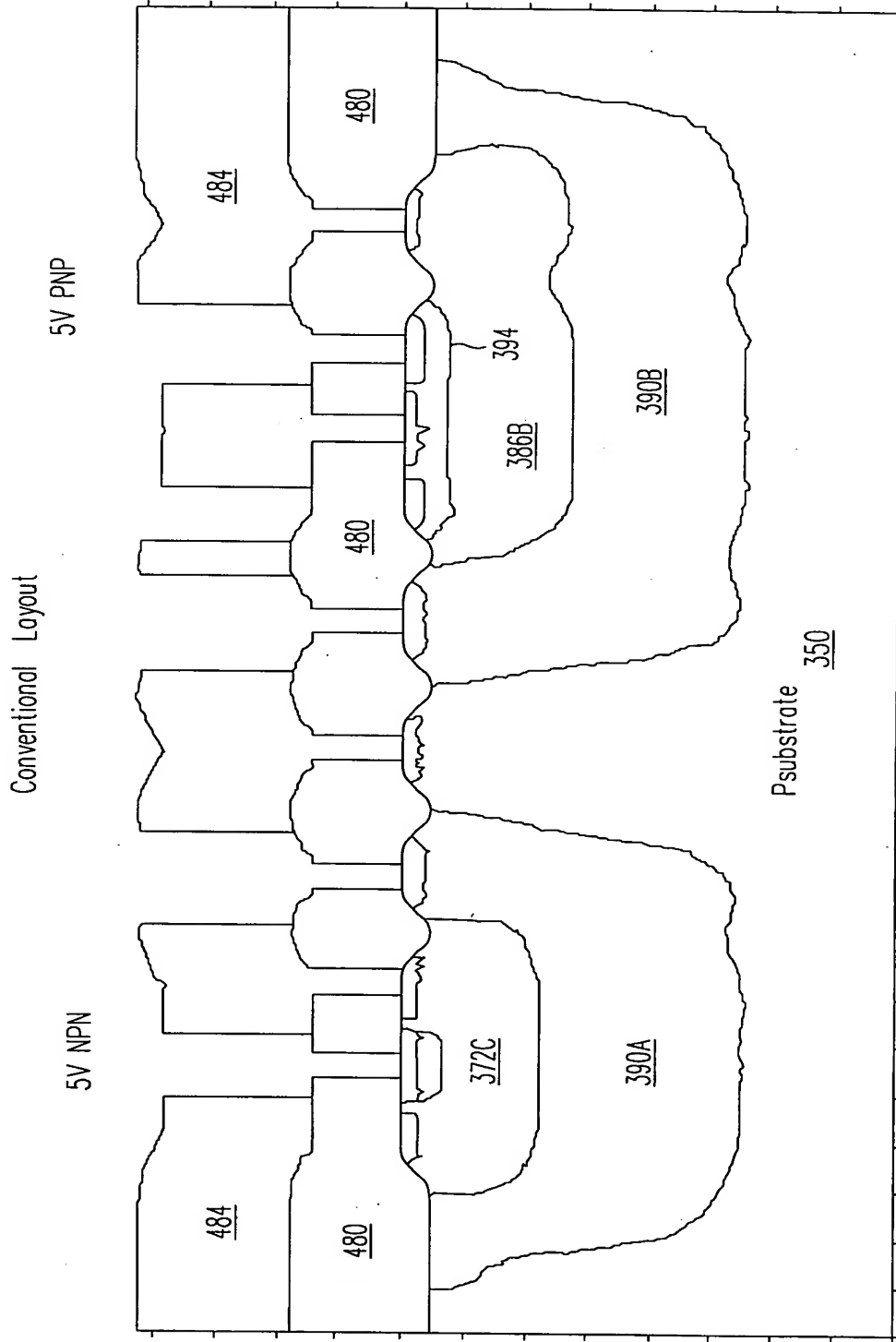
**FIG. 65A**



N-plug Mask and Implant

**FIG. 65B**

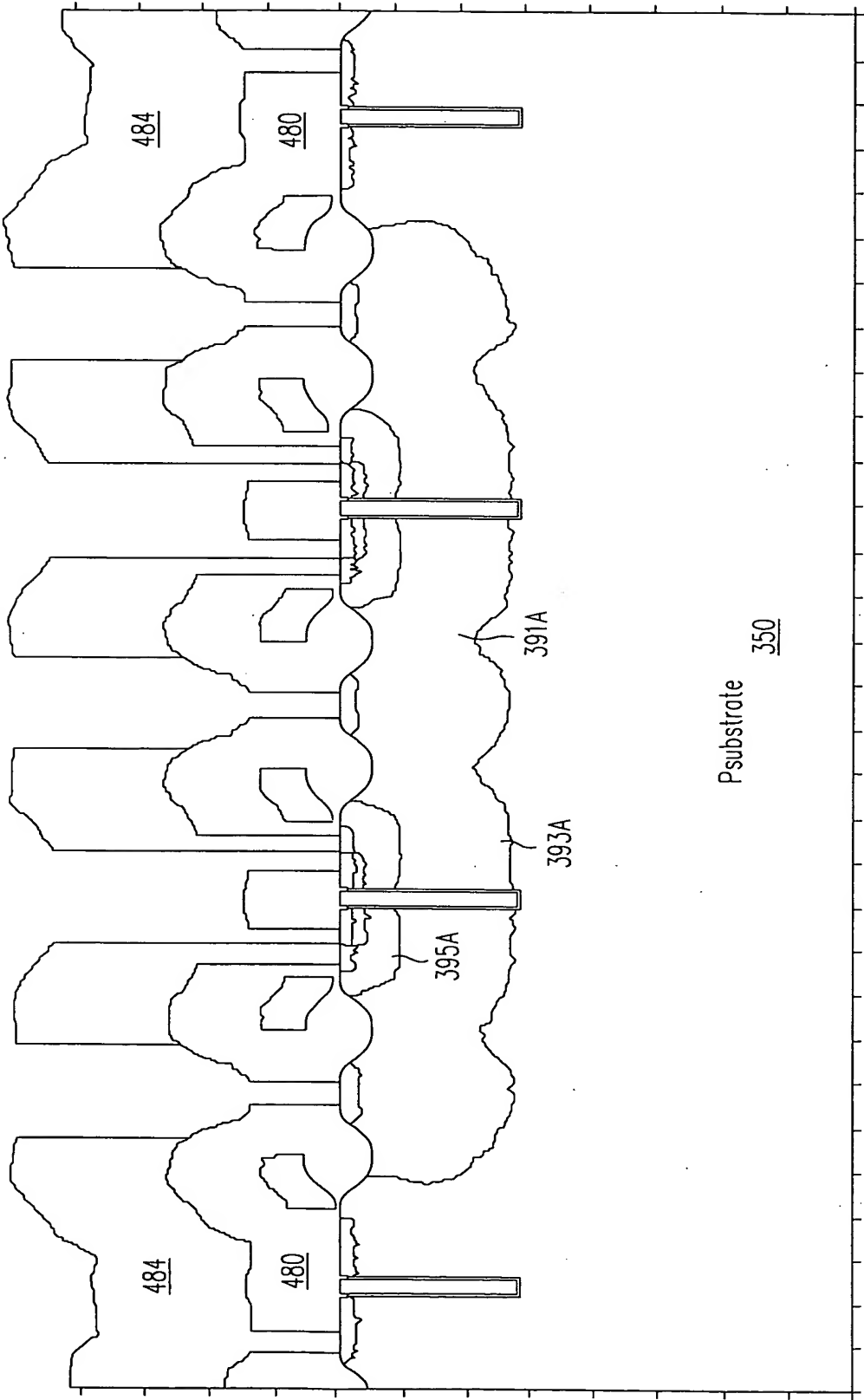




N-plug Mask and Implant

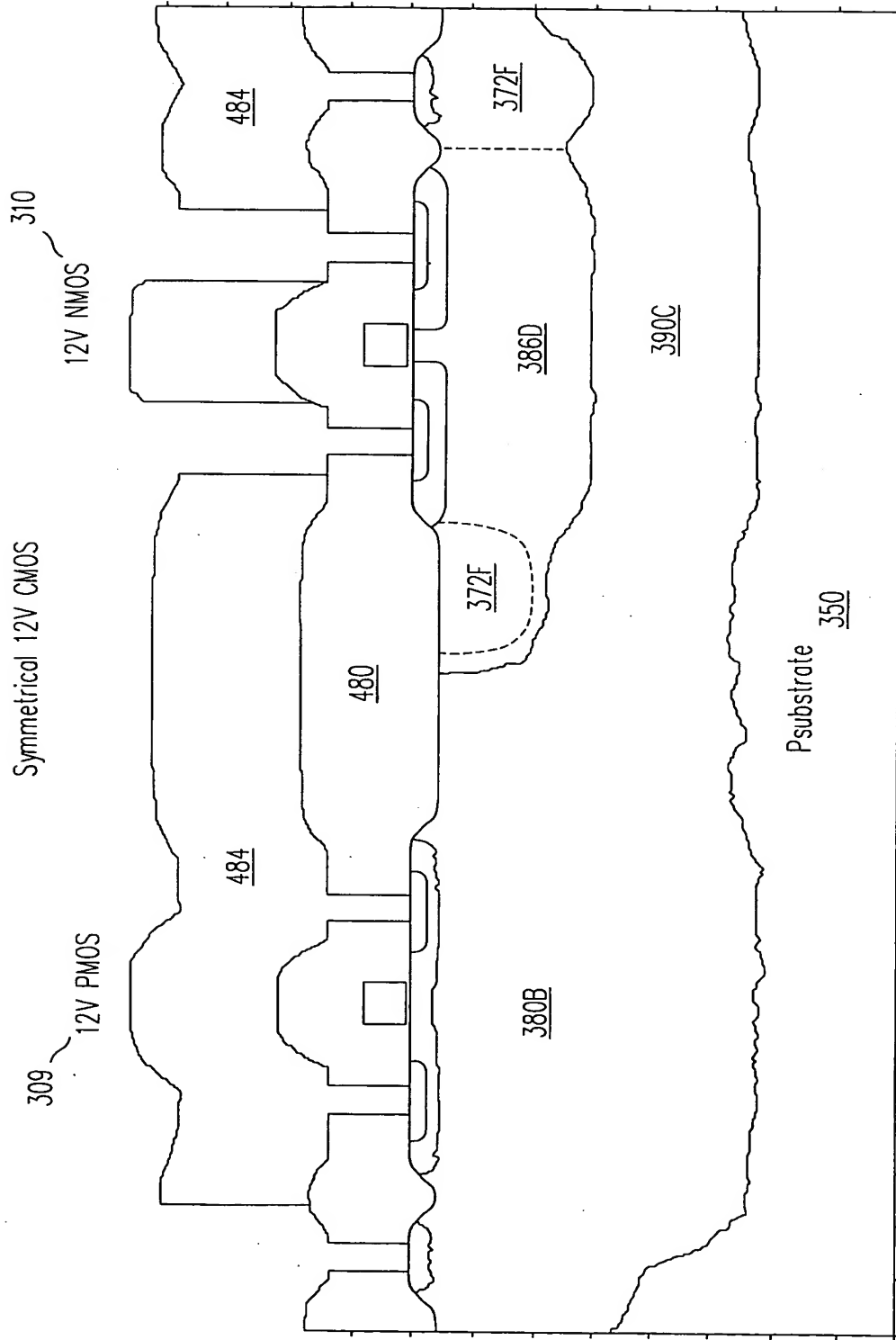
*FIG. 65C*

30V Lateral Trench DMOS ~ 308



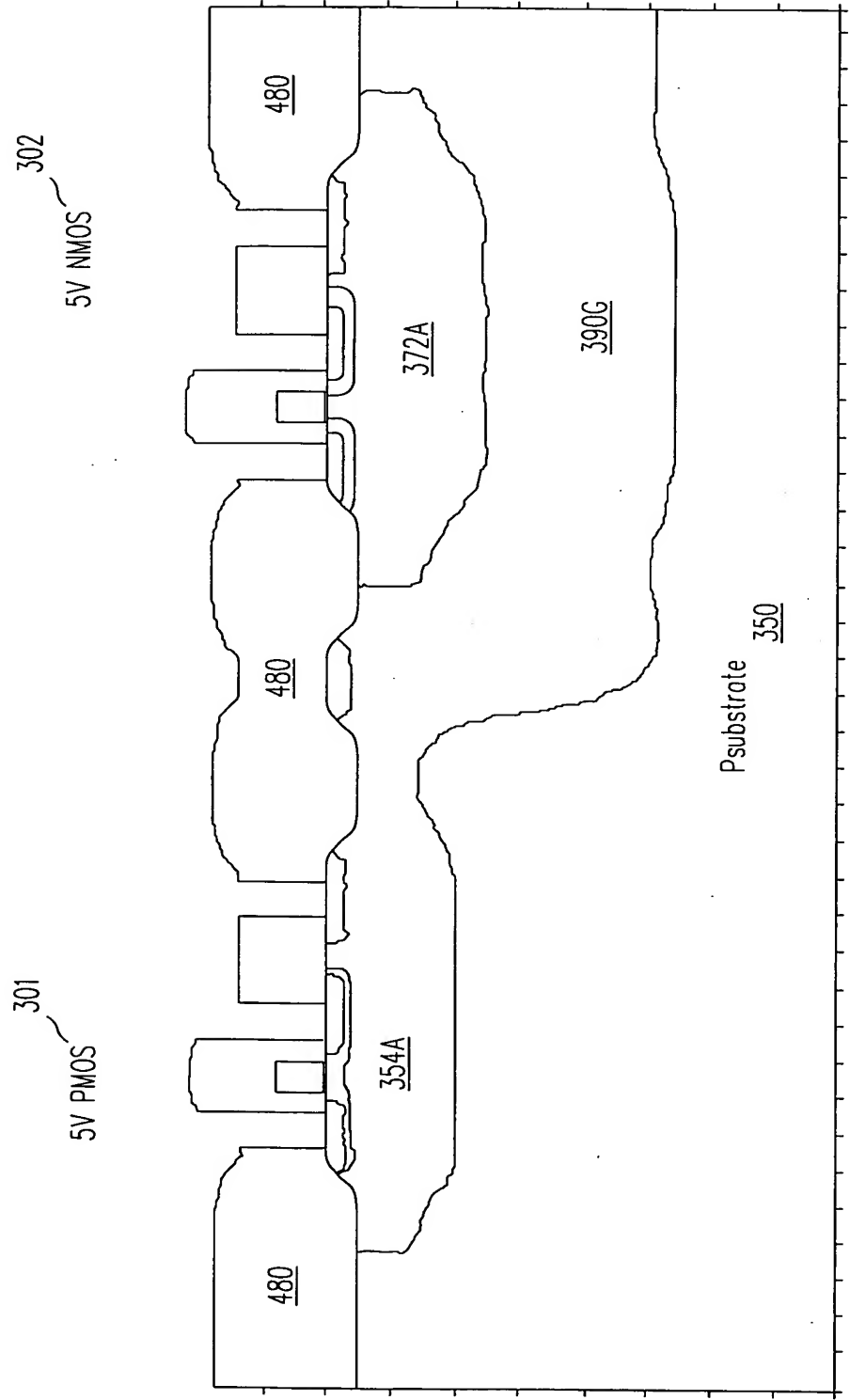
N-plug Mask and Implant

*FIG. 65D*



N-plug Mask and Implant

**FIG. 65E**



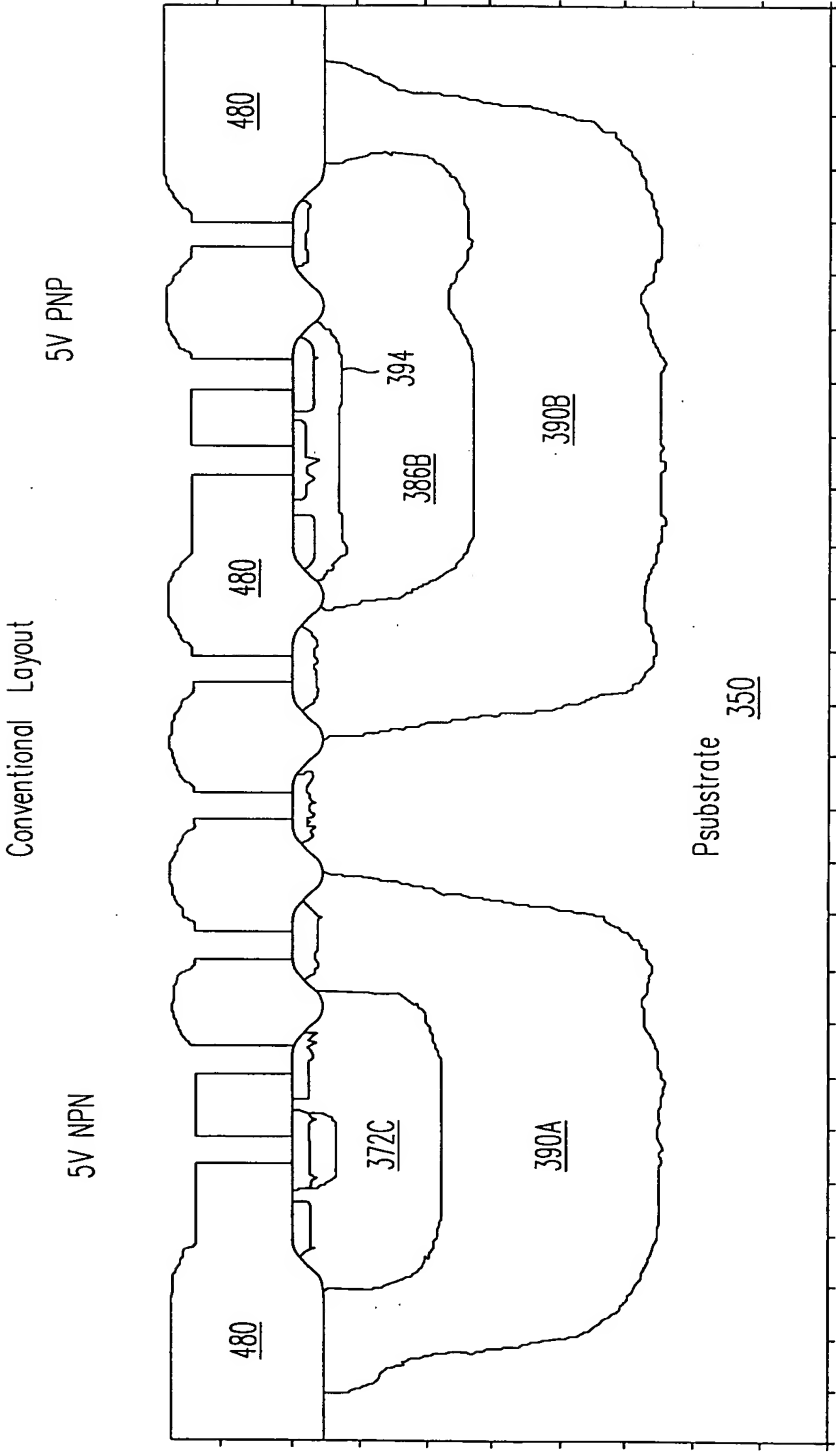
P-plug Implant

**FIG. 66A**



### P-plug Implant

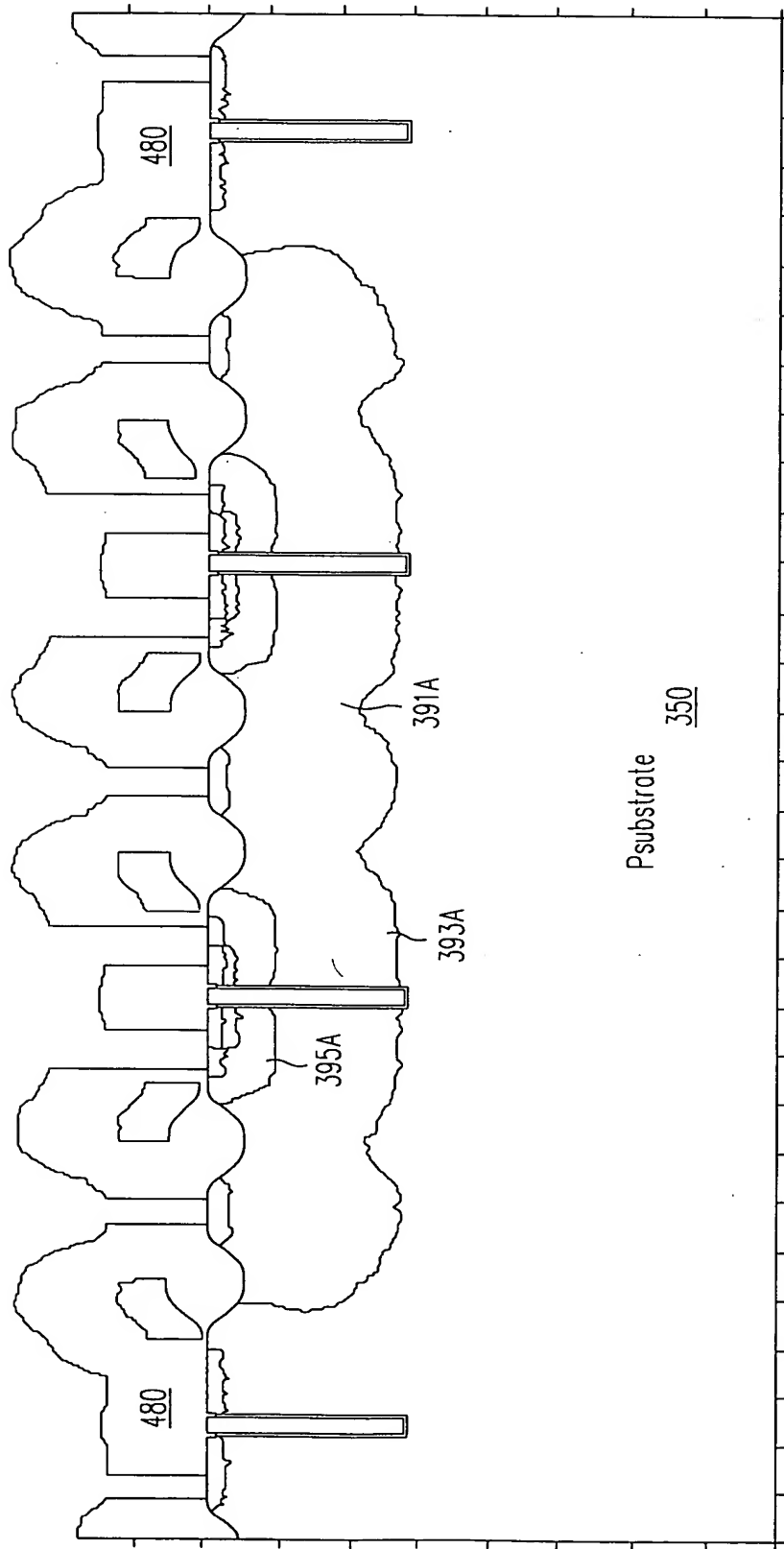
FIG. 66B



P-plug Implant

*FIG. 66C*

30V Lateral Trench DMOS — 308



P-plug Implant

FIG. 66D

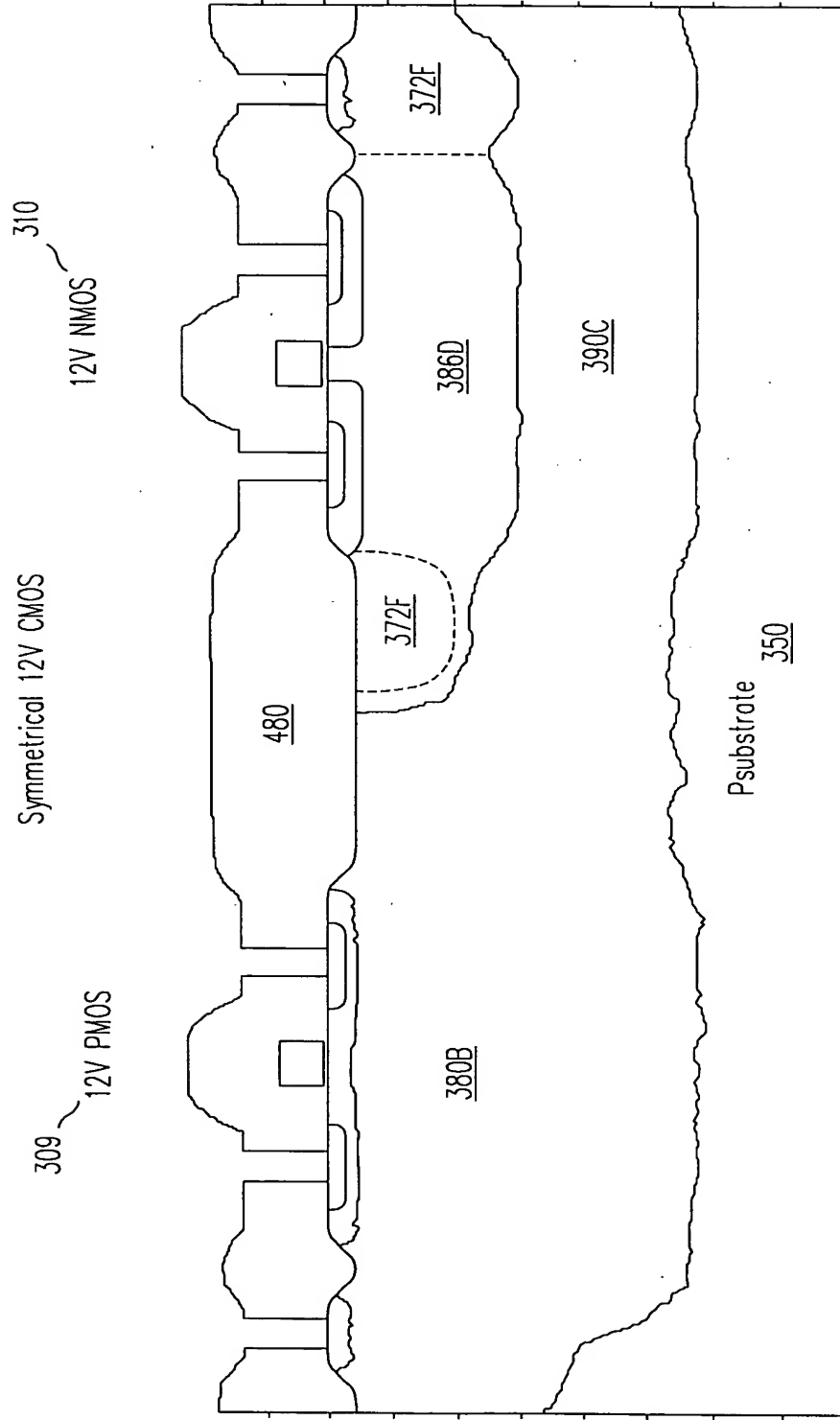


FIG. 66E



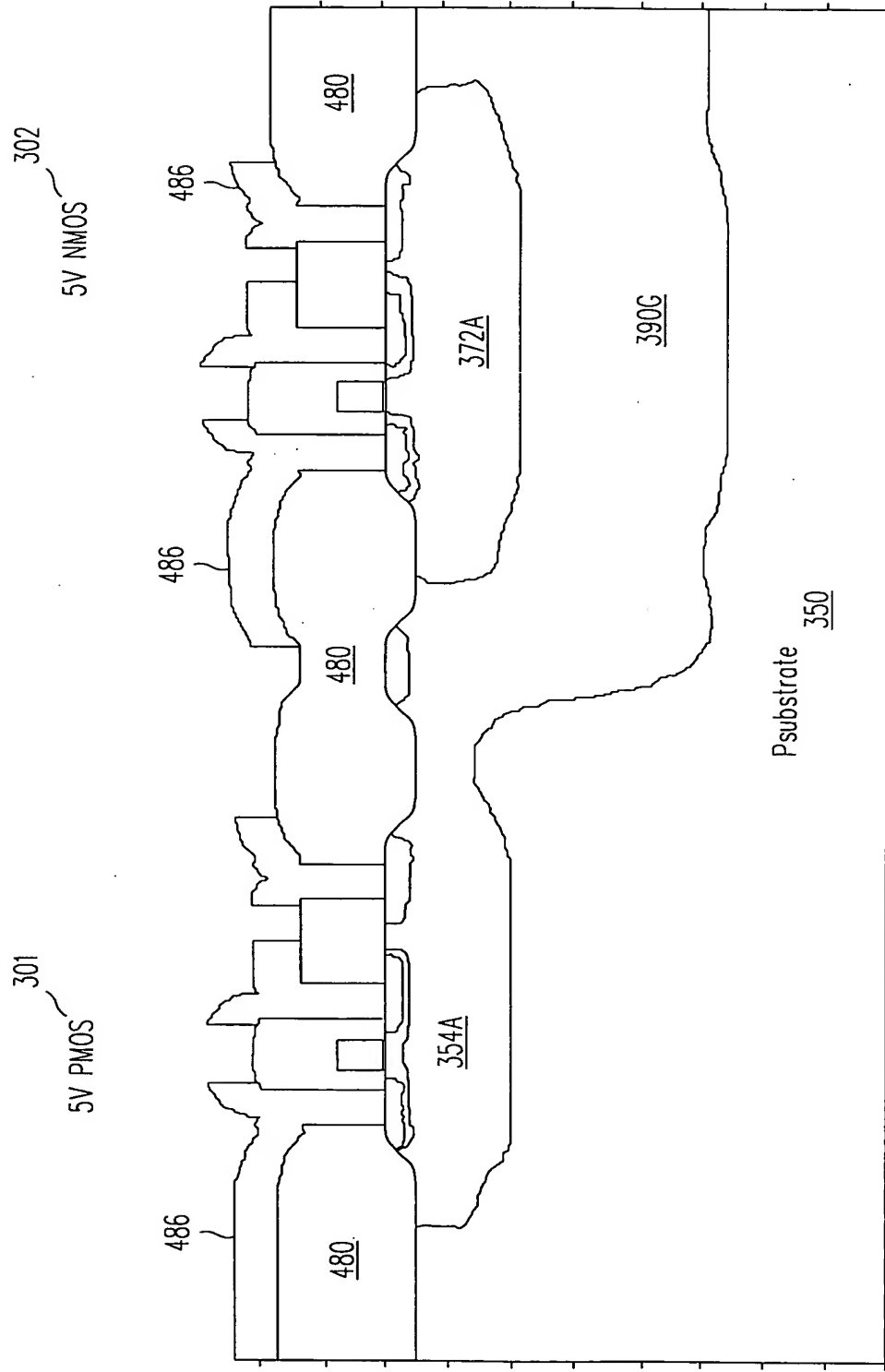


FIG. 67A

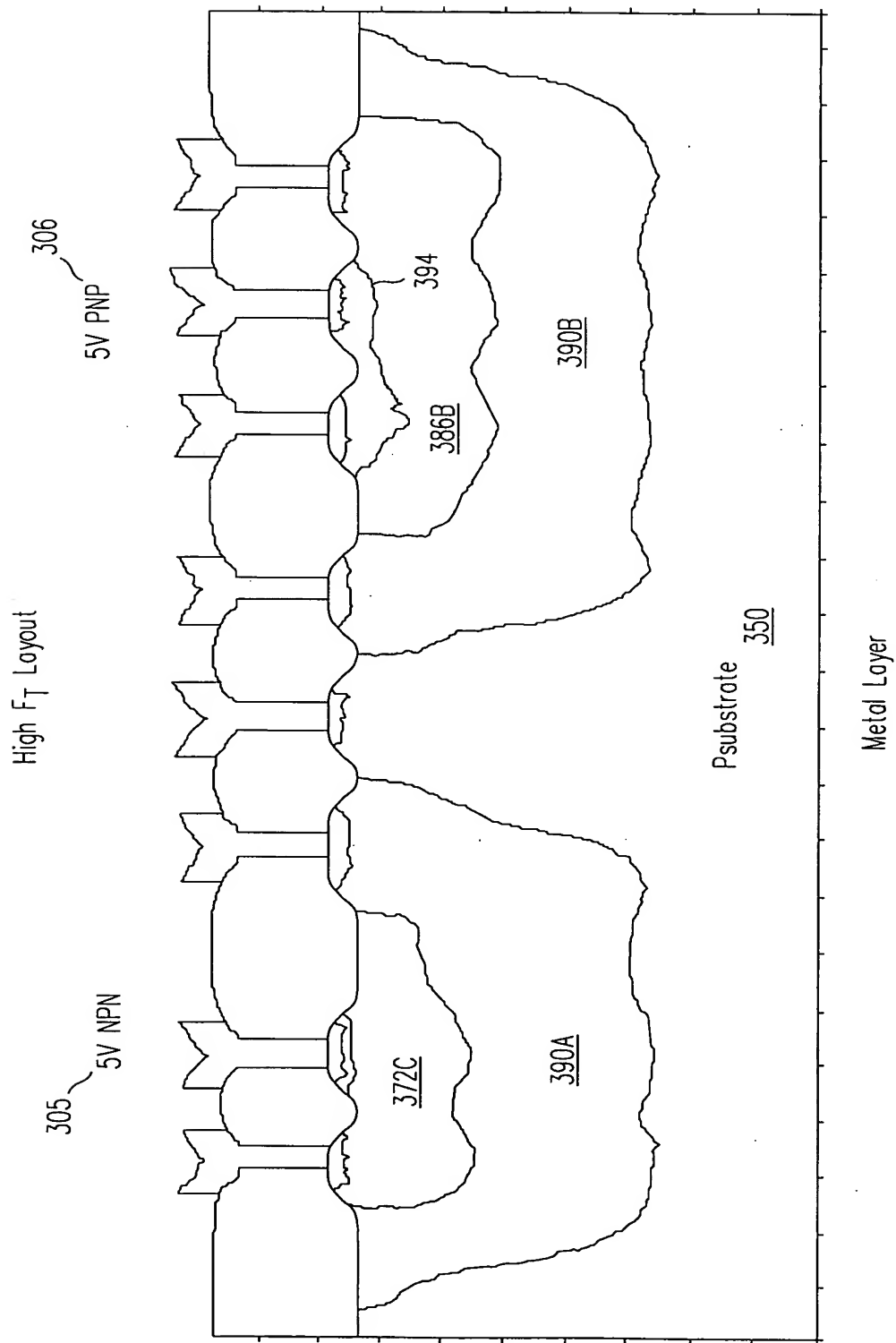


FIG. 67B

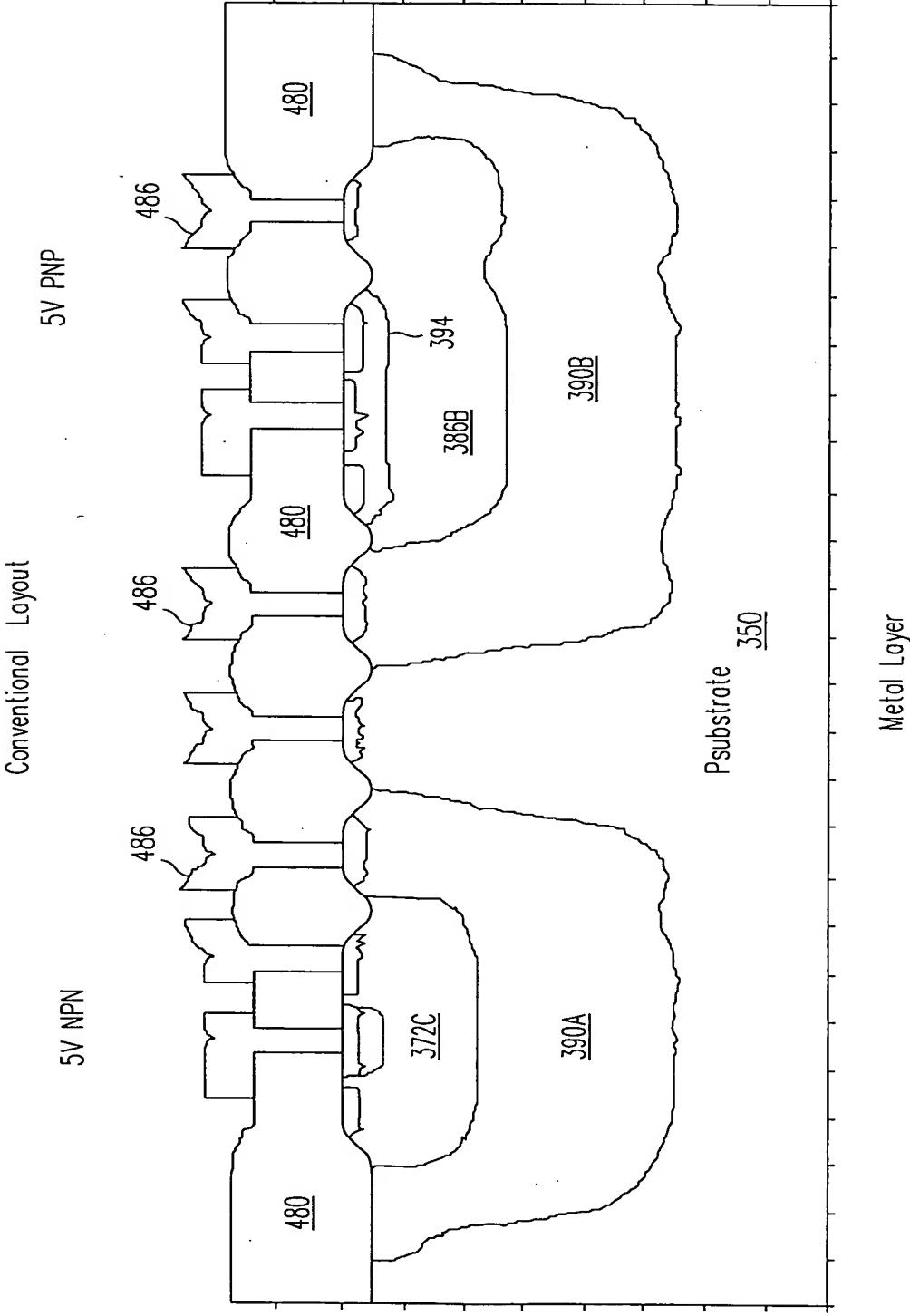
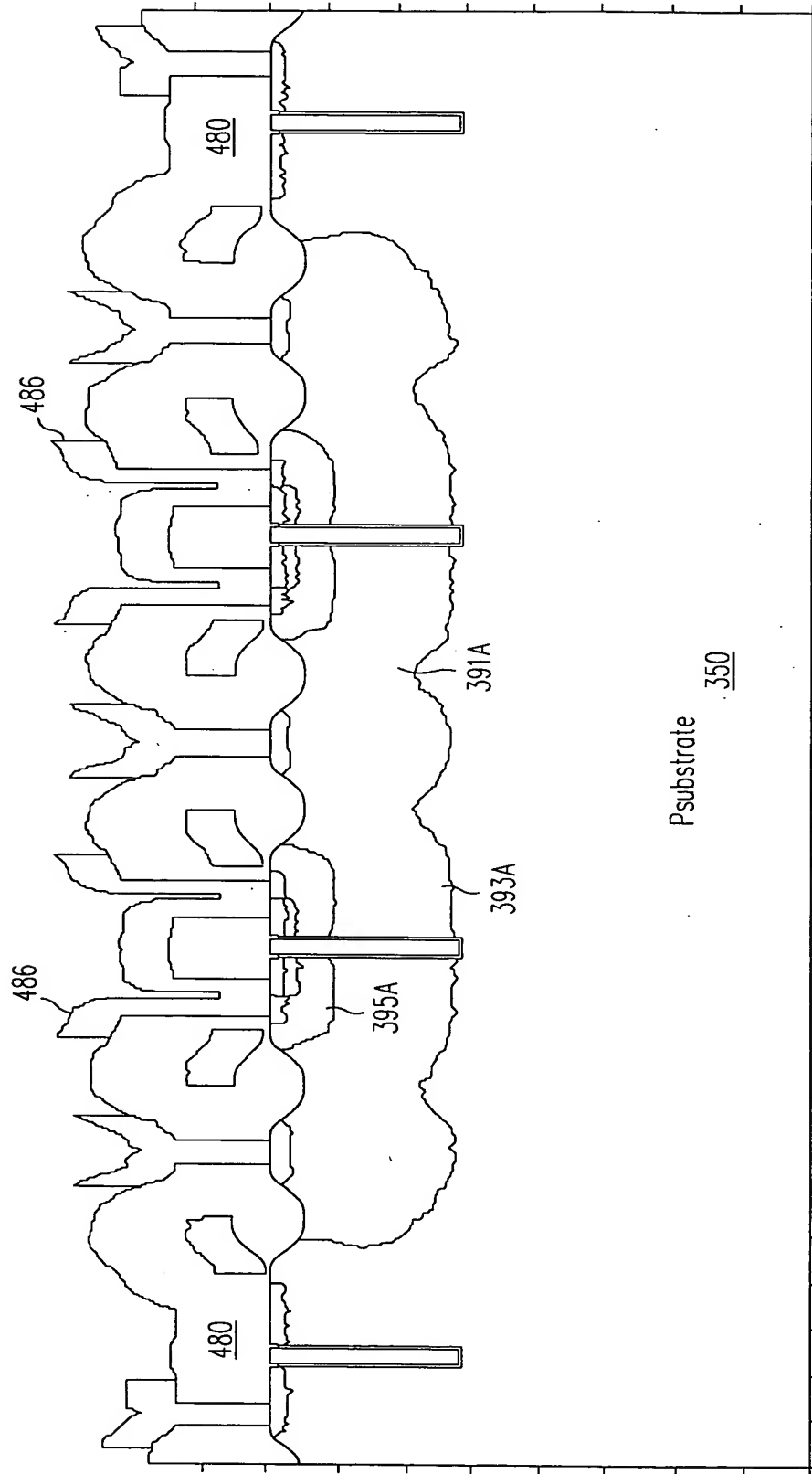


FIG. 67C

30V Lateral Trench DMOS ~ 308



Metal Layer

FIG. 67D

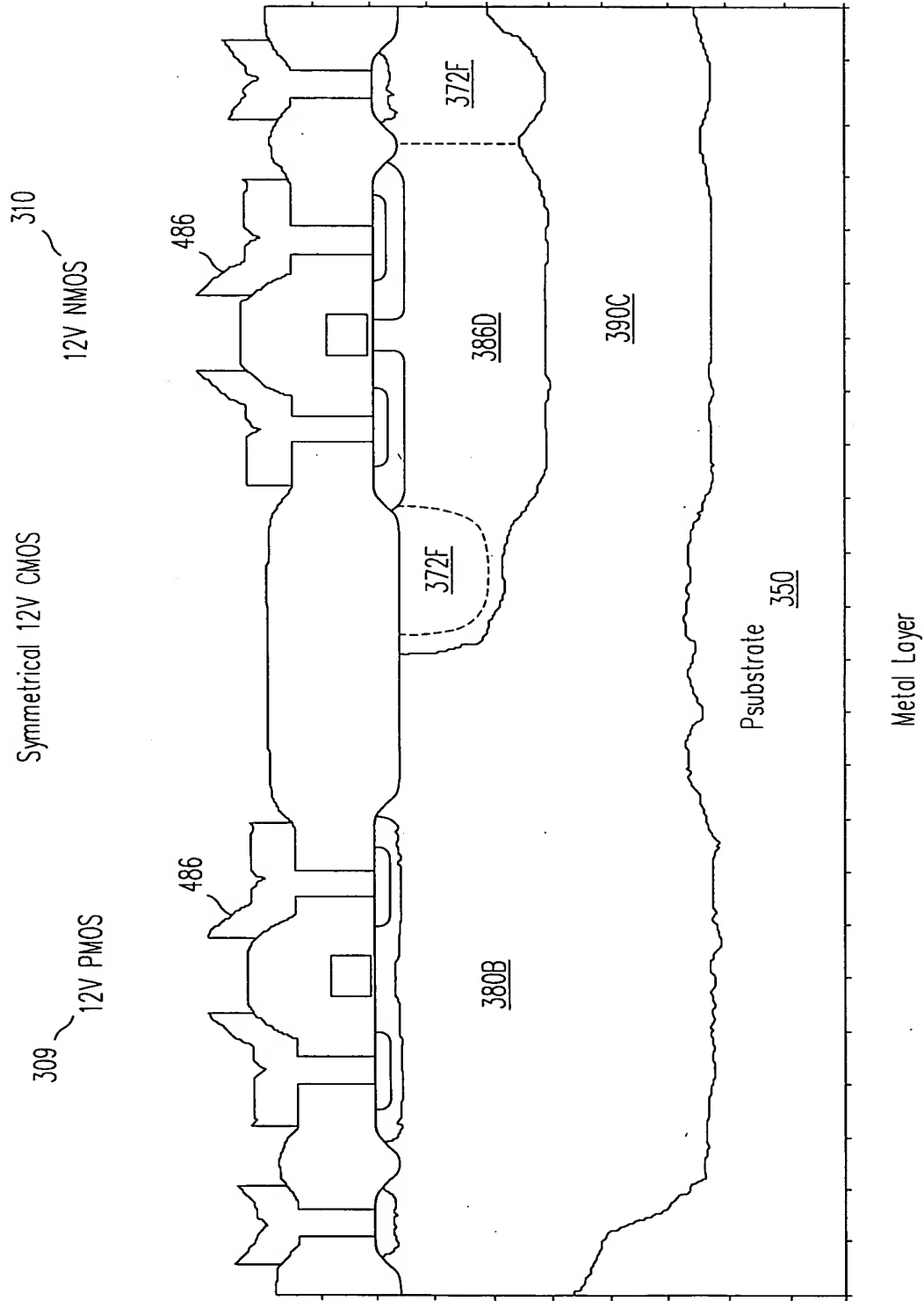


FIG. 67E